Experiment 8
Transistor Characteristics

1 Motivation

Like diodes, transistors are a fundamental element of modern electronics. They are used as amplifiers in signal processing and as voltage-controlled switches. They are the building block for operational amplifier integrated circuits used in a wide array of linear and nonlinear circuit applications. As switches, they are used to construct gates in digital logic circuitry.

2 Background

A transistor is a 3-terminal "active" electronic component, meaning one that behaves as if it has an internal source (current or voltage). There are two main categories of transistors, bipolar-junction (BJT) and field-effect (FET). Each is based on P-N semiconductor junctions. The BJT behaves as a current-controlled current source, and the FET behaves as a voltage-controlled current source. This makes them useful as voltage and current amplifiers. Both can be used as switches. The MOSFET version of the FET has enormous input resistance and is preferred for constructing logic gates.

In this experiment you will investigate the basic properties of the PNP version of the BJT and the N-channel version of the junction field-effect transistor (JFET). The part schematics and package illustrations for these are shown in Fig. 1.

CAUTION! It is easy to get confused when you turn the transistors over to install them in the socket on the circuit board. You are now looking at the top.

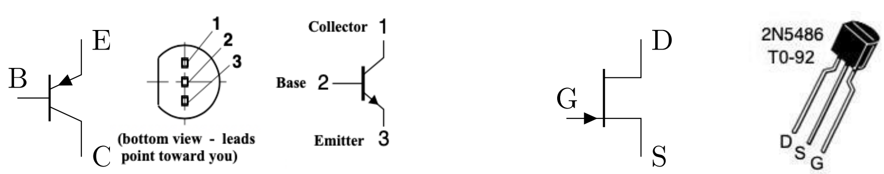

Figure 1: Circuit schematics and lead diagrams for bipolar-junction PNP (2N3906) and N-Channel JFET (2N5486). It is standard to show aa bottom view of the leads for transistors (and vacuum tubes). Perversely, integrated circuits are always shown from the top.

3 Equipment

For this experiment, you will use:

- One Topward dual DC power supply, set for independent supplies (slide switches)
- Two DMM4020 digital multimeters
- Two Keithley digital multimeters
- One circuit board for testing transistors
- One ELC variable resistance box
- One 2N3906 PNP BJT transistor (parts cabinet)
- One 2N5486 N-CHAN JFET transistor (parts cabinet)

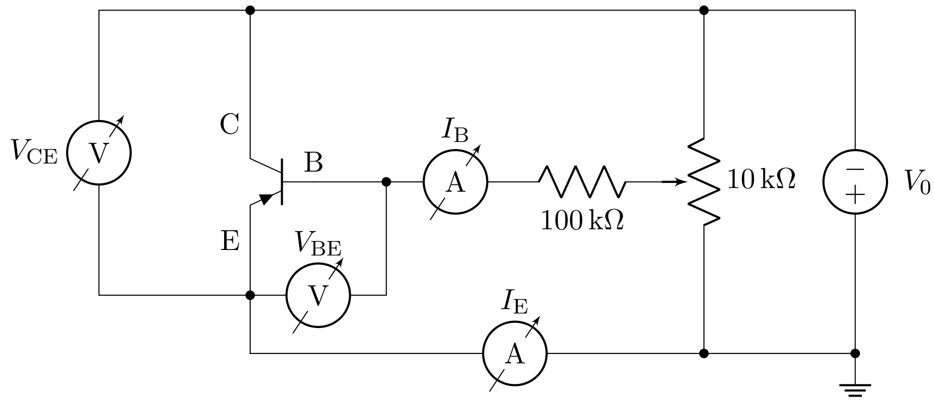

Figure 2: Circuit for characterizing a bipolar junction transistor. Note the polarity of the DC voltage source, which is shown appropriate for a PNP transistor. The polarity would be opposite when working with an NPN transistor.

4 Procedure

1. **The Bipolar Junction Transistor (2N3906):** The schematic for the circuit board for testing transistors is shown in Fig. 2. To complete the circuit, you will first add the four meters shown in the schematic before adding the DC voltage supply. Use a Keithley DMM on the 200 µA scale to measure I_B. Use the other Keithley DMM to measure I_E. Use the two Tektronix DMM's to measure V_{CE} and V_{BE} (via the VΩ HI-LO inputs on the left). **Please be careful setting up the meters!** A current meter has very low (ideally zero) resistance and must be connected in series within a branch of a circuit. If you accidentally place an ammeter across two points in a circuit, the short circut can cause large current to flow that damages components.

   (a) Begin by measuring I_E and V_{BE} as a function of the base current, I_B, for a fixed value of V_{CE}. To do this, complete the circuit as follows: (1) turn the 10 kΩ potentiometer all the way counter-clockwise until the knob stops, which moves the wiper to ground. (2) Connect the ammeters noting their polarity for direction of the current. (3) Connect the voltmeters and the DC voltage supply, being careful to observe polarities. (4) The circuit is mostly prewired (look at the underside of the board), but you need to add one banana patch cable between the terminals for V_0 and the transistor's collector. After double checking your connections, (5) insert the transistor into the socket on the circuit board and then turn on the source and adjust V_0 until $V_{CE} = -12\,\text{V}$.

   (b) Turning the potentiometer will change the base-to-emitter voltage, V_{BE}, and therefore the base current I_B. Measure and tabulate I_E and V_{BE} as a function of I_B. Increase I_B in $2\,\mu\text{A}$ steps from $0 < I_B < 10\,\mu\text{A}$ and then $10\,\mu\text{A}$ steps from $10 < I_B < 50\,\mu\text{A}$. You will notice that V_{BE} drifts slowly when I_B is increased or decreased. This drift is caused by heating of the transistor's P-N junctions, which are sensitive to temperature. Pause briefly after each change in I_B to allow the temperature to stabilize before taking your readings. Calculate β (aka h_{fe}) for your data using $\beta = I_C/I_B$ and make a graph of β versus I_E.

   (c) Measure the input resistance, r_{in} (h_{ie}), as follows: keeping V_{CE} constant (e.g, $V_{CE} = -8\,\text{V}$), set $I_B = 6\,\mu\text{A}$ and measure I_E and V_{BE} then repeat for $I_B = 10\,\mu\text{A}$. Calculate the input resistance using Eq. 1. (A typical value is $h_{ie} = 3.5\,\mathrm{k\Omega}$.)

$$h_{ie} = \left(\frac{\delta V_{\mathrm{BE}}}{\delta I_{\mathrm{B}}}\right)_{V_{\mathrm{CE}}=constant} \tag{1}$$

(d) Table 8.1 in Sprott summarizes a comparison of the models for the "ideal" and "real" transistor with the more complete T-network shown in Fig. 8.5(a). For the "real" transistor, the input resistance, r_{in}, is related to the "transresistance" by $r_{\mathrm{in}} = (\beta+1)r_{tr} \approx \beta r_{tr}$, where $\beta = h_{fe}$ is the current gain. The first row in Table 8.1 gives the equivalents for h_{ie} (the input resistance you found above). In the entry under "T-network", the base resistance, r_{B}, is typically small and can be ignored. Also, since $r_{\mathrm{C}} \gg r_{\mathrm{E}}$, the parallel combination $r_{\mathrm{C}}||r_{\mathrm{E}} \approx r_{\mathrm{E}}$, so $h_{ie} \approx \beta r_{\mathrm{E}}$. In this approximation, the transresistance, r_{tr}, is the same as r_{E}. These are used interchangeably in Sprott's text. Calculate $\beta = h_{fe} = \delta I_{\mathrm{E}}/\delta I_{\mathrm{B}}$ for your measurements in step (c) and then determine r_{tr}. Compare your result with the expected value, $r_{tr} \approx r_d \approx 26\,\mathrm{mV}/\langle I_{\mathrm{E}}\rangle$, where $\langle I_{\mathrm{E}}\rangle$ is the average of the two values from step (c), and r_d is the "dynamic resistance" (Sprott Eq. 8.3).

(e) (*Optional, come back if time remains*) For signal transistors like the 2N3906, the relationship between V_{BE} and I_{E} is given approximately by

$$I_{\mathrm{E}} = I_0\left(e^{eV_{\mathrm{BE}}/kT} - 1\right). \tag{2}$$

The I-V characteristic depends on (absolute) temperature, T, because the electron thermal velocity affects diffusion across the P-N junction. Technically, parameter I_0 also depends on T, but Eq. 2 is a good approximation for fixed T. Make a semi-log plot of I_{E} vs V_{BE} and verify that the low-current region is linear (in semi-log). You can determine eV_{BE}/kT from the slope of a linear fit to your data, assuming that $eV_{\mathrm{BE}}/kT \gg 1$. How does your result compare with the expected value, $e/kT \approx 26\,\mathrm{mV}$ for room temperature? This temperature dependence is interesting physics, but it is rarely important in transistor applications.

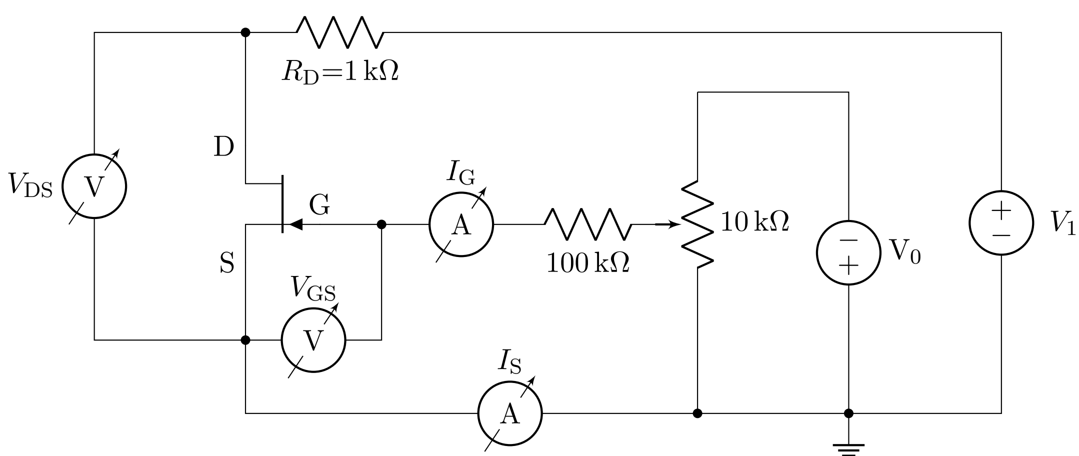

Figure 3: Circuit for characterizing a field-effect transistor. Note the polarity of the DC voltage sources, which are shown appropriate for an N-Channel FET. The polarities would be opposite when testing a P-Channel FET.

2. **The Field-Effect Transistor (2N5486):** You will now measure the properties of an N-channel junction field-effect transistor (JFET). The setup is shown in Fig. 3, which is almost the same as before but with two additions. For a JFET, the potentials between the gate and drain relative to the source have opposite signs, so you need to add a second DC supply, V_1, to provide (positive) voltage at the drain. You also need to add resistor R_D. Note that the lead order of the 2N5486 package is different than the 2N3906 package. (In actual applications, the DC operating point can be established using one DC voltage supply and additional resistors.)

   (a) Make sure you ground the negative terminal of the V_1 supply and the positive terminal of the V_0 supply. The DMMs measure the source current, I_S, the gate current, I_G, and the voltages, V_{DS} and V_{GS}. From Kirchhoff's current rule, the drain current $I_D = I_S - I_G$. After double checking the connections and polarities, turn on the power supplies and set $V_0 = -5\,\mathrm{V}$ and $V_1 = 0\,\mathrm{V}$.

   (b) An FET can be used as a voltage-controlled variable resistor. The resistance of the drain-source channel is adjusted by varying the gate voltage, V_{GS}. (Internally this changes the width of the depletion region.) Turn the potentiometer fully CCW so that $V_{GS} = 0$. Now vary V_{DS} (by adjusting V_1) from $0\,\mathrm{V}$ to $+2.0\,\mathrm{V}$ in $0.2\,\mathrm{V}$ steps and from $+2.0\,\mathrm{V}$ to $+10.0\,\mathrm{V}$ in $2.0\,\mathrm{V}$ steps. You should see that I_G is always very small, hence $I_D = I_S$. Why is I_G small? Tabulate your data and make a plot of I_D versus V_{DS}. Determine the resistance of the drain-source channel, R_{DS}, from the ohmic (linear) region of the plot.

   (c) Now measure the characteristics of the JFET in the "pinch-off" region where I_D is nearly independent of V_{DS}, i.e., the transistor acts like a current source. This is the region where a JFET is used as an amplifier. Set $V_{GS} = -1.5\,\mathrm{V}$ by adjusting the potentiometer, and then vary V_{DS} from $+2.0\,\mathrm{V}$ to $+20\,\mathrm{V}$ in $2.0\,\mathrm{V}$ steps. Tabulate your data and make a plot of I_D versus V_{DS}.

   (d) In the "pinch-off" region, the JFET behaves like a voltage-controlled current source. Use your data from steps (b) and (c) for $V_{DS} = +10\,\mathrm{V}$ to determine the "forward transconductance". (A typical value is $g_{fs} = 5\,\mathrm{m}\mho$.)

$$g_{fs} = \left(\frac{\delta I_D}{\delta V_{GS}}\right)_{V_{DS}=constant} \tag{3}$$

   (e) As a nearly ideal current source, a JFET has a large but finite output resistance, r_{os} (see the equivalent circuit in Sprott Fig. 7.16). Evalutate the output resistance in the pinch-off region, $r_{os} = \delta V_{DS}/\delta I_D$, using your measurements from step (c) with $V_{DS} = +10\,\mathrm{V}$ and $+20\,\mathrm{V}$.

   (f) FET's (usually MOSFETs) are very useful as switches and gates. The "switch" is closed when $V_{GS} = 0$ and open when $|V_{GS}| > |V_P|$, the critical pinch-off voltage (also called $V_{GS(off)}$). With $V_{DS} = +12\,\mathrm{V}$, vary the potentiometer to change the gate-source voltage, V_{GS}. Measure and tabulate I_D as a function of V_{DS} by varying $V_{GS} = 0\,\mathrm{V}$ in $-0.5\,\mathrm{V}$ steps up to the critical pinch-off voltage. (You can adjust V_1 to maintain $V_{DS} = +12\,\mathrm{V}$.) Plot I_D versus V_{GS} and determine the "off" voltage for the JFET. The plot should look roughly parabolic as V_{GS} approaches V_P.

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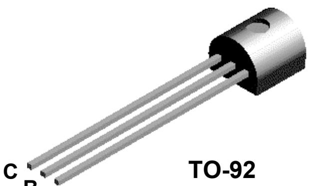
2N3906 MMBT3906 PZT3906



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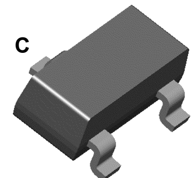

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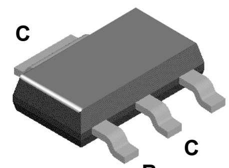


SOT-223

PNP General Purpose Amplifier

This device is designed for general purpose amplifier and switching applications at collector currents of 10 μA to 100 mA.

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	-40	V
V_{CBO}	Collector-Base Voltage	-40	V
V_{EBO}	Emitter-Base Voltage	-5.0	V
I_C	Collector Current - Continuous	-200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3906	***MMBT3906**	****PZT3906**	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

**Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

PNP General Purpose Amplifier
(continued)

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage*	I_C = -1.0 mA, I_B = 0	-40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = -10 μA, I_E = 0	-40		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = -10 μA, I_C = 0	-5.0		V
I_{BL}	Base Cutoff Current	V_{CE} = -30 V, V_{BE}= -3.0 V		-50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = -30 V, V_{BE}= -3.0 V		-50	nA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain *	I_C = -0.1 mA, V_{CE}= -1.0 V I_C = -1.0 mA, V_{CE}= -1.0 V I_C = -10 mA, V_{CE}= -1.0 V I_C = -50 mA, V_{CE}= -1.0 V I_C = -100 mA, V_{CE}= -1.0 V	60 80 100 60 30	 300 	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = -10 mA, I_B = -1.0 mA I_C = -50 mA, I_B = -5.0 mA		-0.25 -0.4	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = -10 mA, I_B = -1.0 mA I_C = -50 mA, I_B = -5.0 mA	-0.65	-0.85 -0.95	V V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = -10 mA, V_{CE} = -20 V, f = 100 MHz	250		MHz
C_{obo}	Output Capacitance	V_{CB} = -5.0 V, I_E = 0, f = 100 kHz		4.5	pF
C_{ibo}	Input Capacitance	V_{EB} = -0.5 V, I_C = 0, f = 100 kHz		10.0	pF
NF	Noise Figure	I_C = -100 μA, V_{CE} = -5.0 V, R_S =1.0 kΩ, f=10 Hz to 15.7 kHz		4.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = -3.0 V, V_{BE}= -0.5 V,		35	ns
t_r	Rise Time	I_C = -10 mA, I_{B1}= -1.0 mA		35	ns
t_s	Storage Time	V_{CC} = -3.0 V, I_C = -10 mA		225	ns
t_f	Fall Time	I_{B1} = I_{B2} = -1.0 mA		75	ns

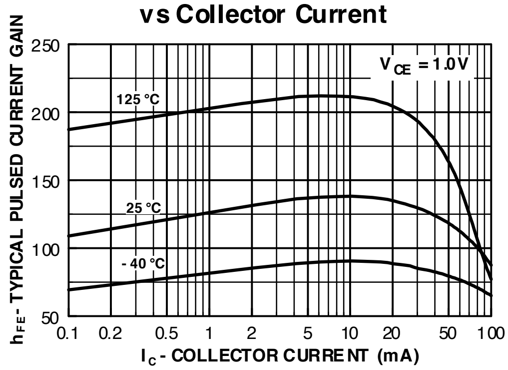
*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Spice Model

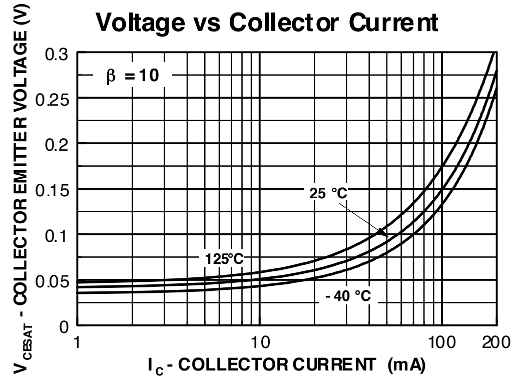
PNP (Is=1.41f Xti=3 Eg=1.11 Vaf=18.7 Bf=180.7 Ne=1.5 Ise=0 Ikf=80m Xtb=1.5 Br=4.977 Nc=2 Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p Mjc=.5776 Vjc=.75 Fc=.5 Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n Tf=179.3p Itf=.4 Vtf=4 Xtf=6 Rb=10)

Typical Characteristics

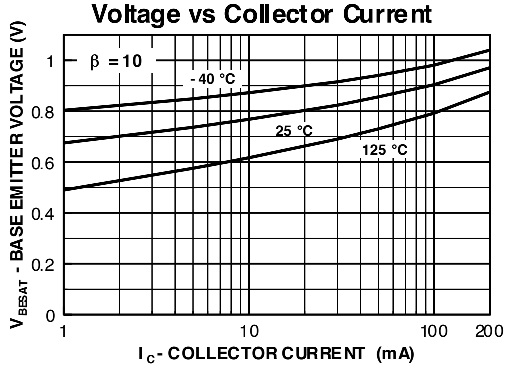
Typical Pulsed Current Gain vs Collector Current



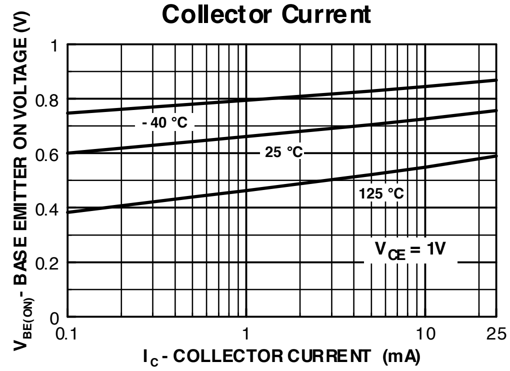
Collector-Emitter Saturation Voltage vs Collector Current



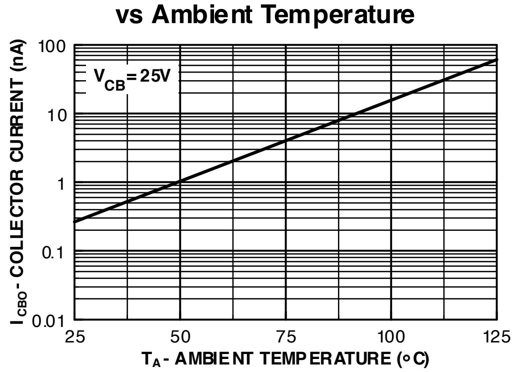
Base-Emitter Saturation Voltage vs Collector Current



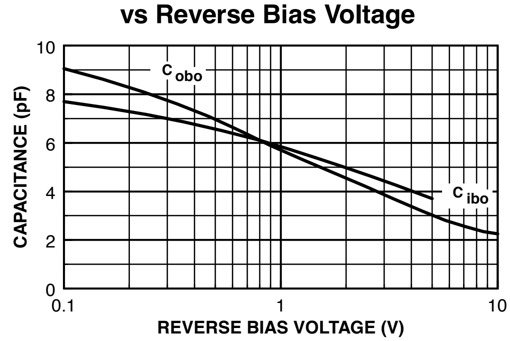
Base Emitter ON Voltage vs Collector Current



Collector-Cutoff Current vs Ambient Temperature



Common-Base Open Circuit Input and Output Capacitance vs Reverse Bias Voltage



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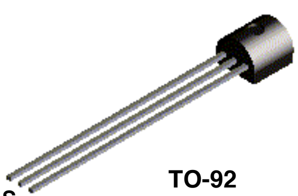
Discrete POWER & Signal Technologies

2N5484 2N5485 2N5486 MMBF5484 MMBF5485 MMBF5486



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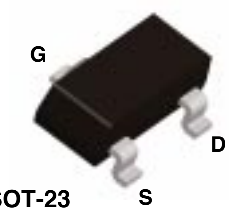

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SOT-23
Mark: 6B / 6M / 6H

N-Channel RF Amplifier

This device is designed primarily for electronic switching applications such as low On Resistance analog switching. Sourced from Process 50.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	- 25	V
I_{GF}	Forward Gate Current	10	mA
T_J ,T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

TA = 25°C unless otherwise noted

Symbol	Characteristic	Max		Units
		2N5484	*MMBF5484	
P_D	Total Device Dissipation Derate above 25°C	350 2.8	225 1.8	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

N-Channel RF Amplifier
(continued)

Electrical Characteristics
TA = 25°C unless otherwise noted

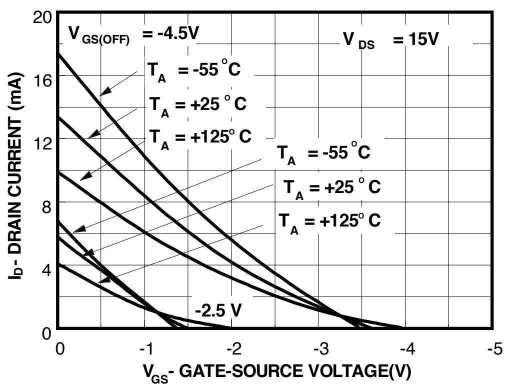
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	I_G = - 1.0 μA, V_{DS} = 0	- 25			V
I_{GSS}	Gate Reverse Current	V_{GS} = - 20 V, V_{DS} = 0			- 1.0	nA
		V_{GS} = - 20 V, V_{DS} = 0, T_A = 100°C			- 0.2	μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15 V, I_D = 10 nA **2N5484**	- 0.3		- 3.0	V
		2N5485	- 0.5		- 4.0	V
		2N5486	- 2.0		- 6.0	V
ON CHARACTERISTICS						
I_{DSS}	Zero-Gate Voltage Drain Current*	V_{DS} = 15 V, V_{GS} = 0 **2N5484**	1.0		5.0	mA
		2N5485	4.0		10	mA
		2N5486	8.0		20	mA
SMALL SIGNAL CHARACTERISTICS						
g_{fs}	Forward Transfer Conductance	V_{DS} = 15, V_{GS} = 0, f = 1.0 kHz				
		2N5484	3000		6000	μmhos
		2N5485	3500		7000	μmhos
		2N5486	4000		8000	μmhos
$Re(y_{is})$	Input Conductance	V_{DS} = 15, V_{GS} = 0, f = 100 MHz				
		2N5484			100	μmhos
		V_{DS} = 15, V_{GS} = 0, f = 400 MHz				
		2N5485 / 2N5486			1000	μmhos
g_{os}	Output Conductance	V_{DS} = 15, V_{GS} = 0, f = 1.0 kHz				
		2N5484			50	μmhos
		2N5485			60	μmhos
		2N5486			75	μmhos
$Re(y_{os})$	Output Conductance	V_{DS} = 15, V_{GS} = 0, f = 100 MHz				
		2N5484			75	μmhos
		V_{DS} = 15, V_{GS} = 0, f = 400 MHz				
		2N5485 / 2N5486			100	μmhos
$Re(y_{fs})$	Forward Transconductance	V_{DS} = 15, V_{GS} = 0, f = 100 MHz				
		2N5484	2500			μmhos
		V_{DS} = 15, V_{GS} = 0, f = 400 MHz				
		2N5485	3000			μmhos
		2N5486	3500			μmhos
C_{iss}	Input Capacitance	V_{DS} = 15, V_{GS} = 0, f = 1.0 MHz			5.0	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15, V_{GS} = 0, f = 1.0 MHz			1.0	pF
C_{oss}	Output Capacitance	V_{DS} = 15, V_{GS} = 0, f = 1.0 MHz			2.0	pF
NF	Noise Figure	V_{DS}= 15 V, R_G = 1.0 kΩ, f = 100 MHz **2N5484**			3.0	dB
		V_{DS}= 15 V, R_G = 1.0 kΩ, f = 400 MHz **2N5484**		4.0		dB
		V_{DS}= 15 V , R_G = 1.0 kΩ, f = 100 MHz **2N5485 / 2N5486**			2.0	dB
		V_{DS}= 15 V, R_G = 1.0 kΩ, f = 400 MHz **2N5485 / 2N5486**			4.0	dB

*Pulse Test: Pulse Width £ 300 ms, Duty Cycle £ 2%

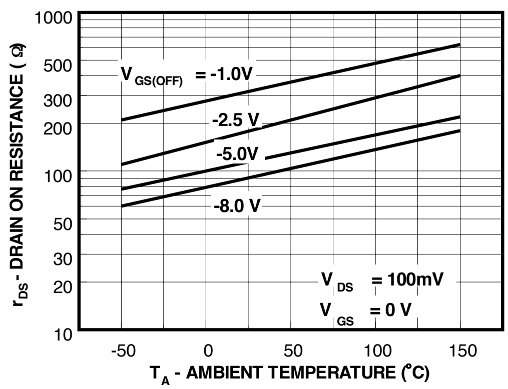
N-Channel RF Amplifier
(continued)

Typical Characteristics

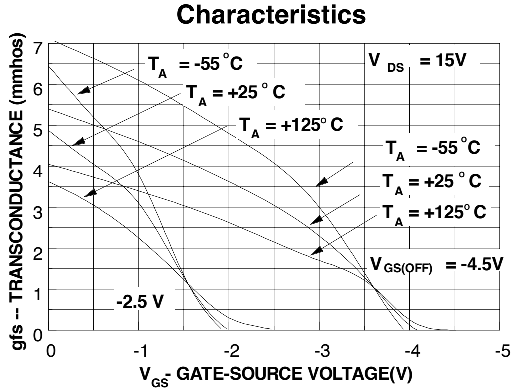
Transfer Characteristics



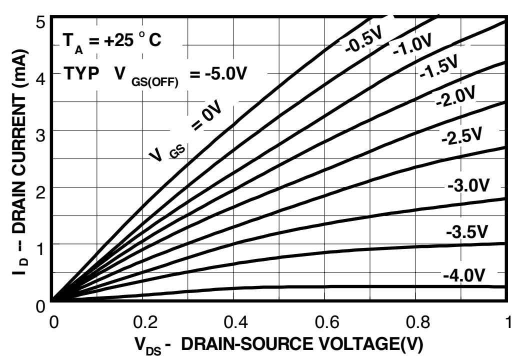
Channel Resistance vs Temperature



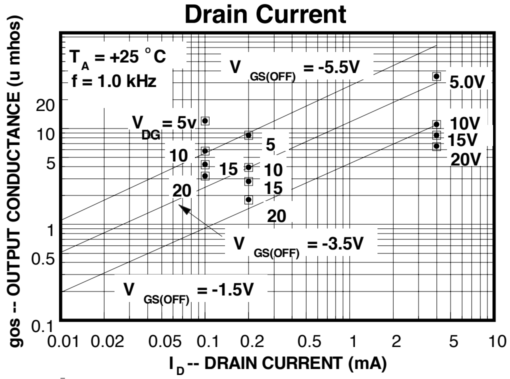
Transconductance Characteristics



Common Drain-Source Characteristics



Output Conductance vs Drain Current



Transconductance Parameter Interactions