

technical information manual

NIM MODEL 364AL/365AL

DUAL 4-FOLD MAJORITY LOGIC

GATE WITH VETO

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

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**See pocket in back of manual for schematics,
parts lists, and additional addenda with any
changes to manual.**

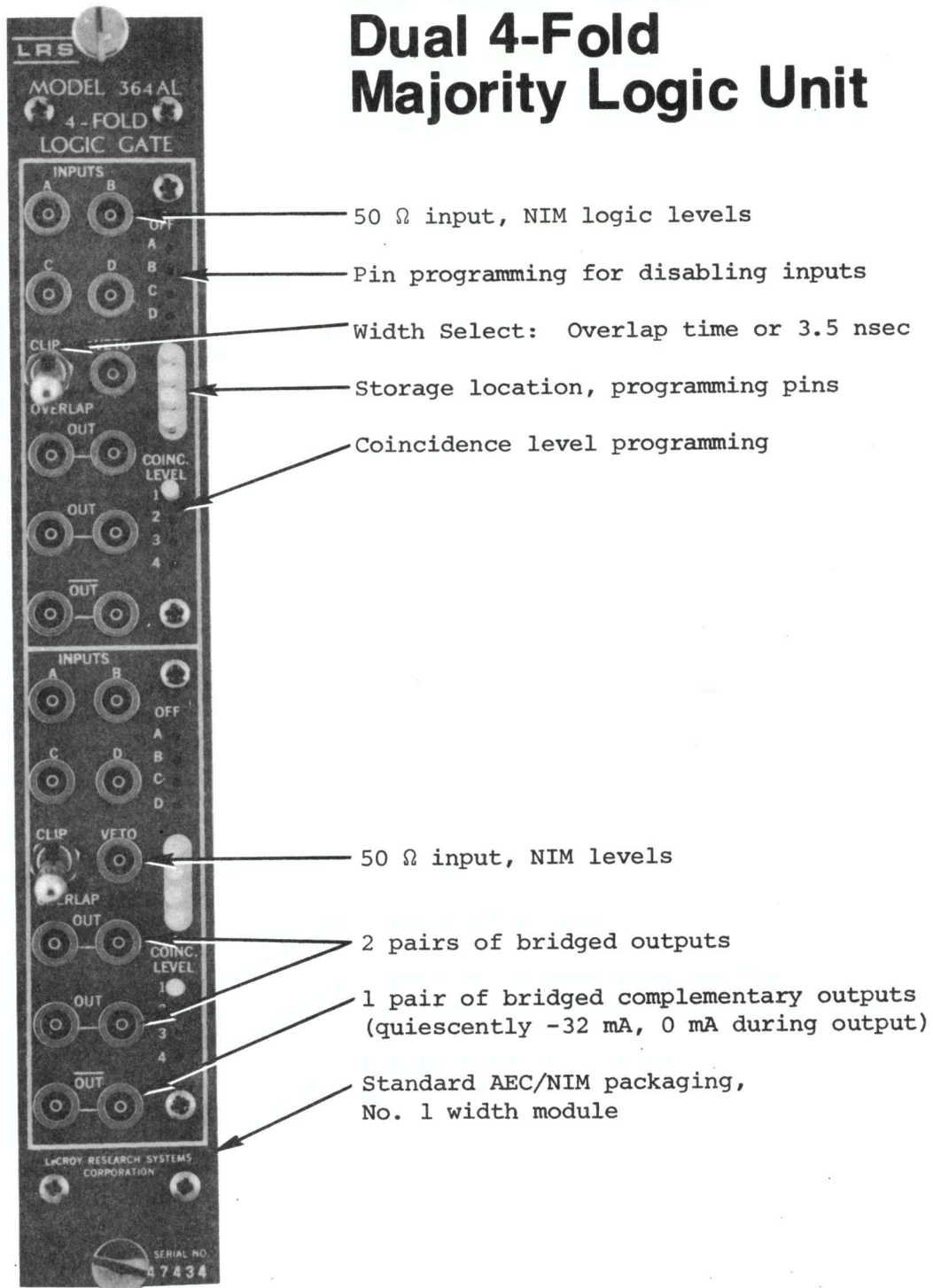
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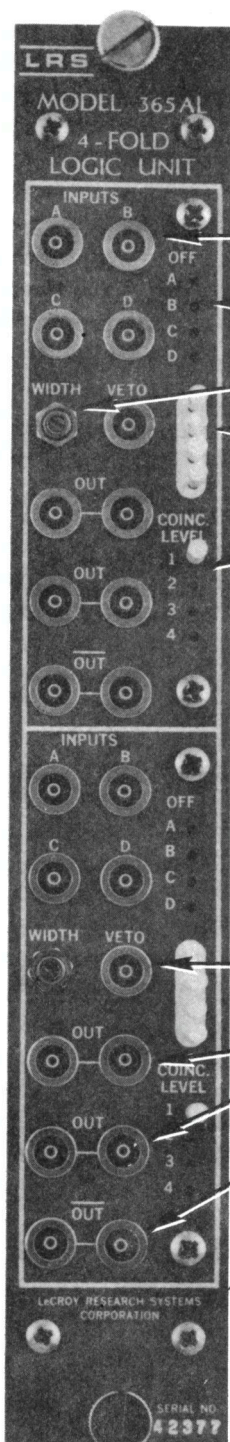
September, 1979

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

NIM Model 364AL Dual 4-Fold Majority Logic Unit



NIM Model 365AL Dual 4-Fold Majority Logic Unit



50 Ω input, NIM logic levels

Pin programming for disabling inputs

Continuous width adjust, 4 ns - 50 ns

Storage location, programming pins

Coincidence level programming

50 Ω input, NIM levels

2 pairs of bridged outputs

1 pair of bridged complementary outputs
(quiescently -32 mA, 0 mA during output)

Standard AEC/NIM packaging,
No. 1 width module

GENERAL DESCRIPTION

The Model 364 AL and 365 AL are dual 4-fold logic gates which offer the functions of fan-in, coincidence, leading edge inhibit, majority logic, and pulse standardization. Each of two identical channels accepts standard NIM logic signals at each of the four logic inputs and one veto input. All inputs are terminated in 50Ω . Lemo-type connectors are used.

A front-panel selector allows programming the number of simultaneous negative inputs required for an output. With its majority logic capability, the unit may be used to perform voter coincidence such as 1 of 1, 2, 3, 4 (logic fan-in), 2 of 3, 4, or 3 of 4 as well as the standard coincidences of 2 of 2, 3 of 3, 4 of 4. Any of the input serves as an inhibit input when driven with a complementary logic signal. A separate veto input is provided for inhibiting the output regardless of the state of other inputs.

Both channels of the 364 AL and 365 AL may be gated off by means of the NIM bin gate. The bin gate enters the module via the rear multipin power connector and a rear-panel On-Off switch. Quiescently at +5 volts, the bin gate must be clamped to ground to inhibit the logic unit. The bin gate is direct-coupled, and has rise and fall times of approximately 50 ns for the 365 AL and 20 nsec for the 364 AL.

A front-panel selector is provided for programming the participating inputs. Inserting the programming pins in any of the designated Off positions disables that input and eliminates the necessity of removing input cables. A separate storage location is provided for holding the programming pins not in use.

Once the input coincidence conditions have been satisfied, the Model 364 AL and 365 AL generates three double-amplitude NIM fast logic outputs. Each output is provided with two paralleled connectors to enable the signal to be clipped, back-terminated, or fanned-out to two 50Ω loads. The positive output, or complement ($\overline{\text{OUT}}$) is quiescently at a logical one state (-32 mA) and switches to 0 mA (or 0 volts) for the duration of the output. The two negative outputs (OUT) are quiescently at zero and switch to -32 mA (-800 mV if both connectors drive 50Ω loads) during an output.

The output duration of each channel of the 364 AL is either the time overlap of the signals satisfying the coincidence conditions, or a fixed 3.5 ns.

The output duration of each channel of the 365 AL is adjustable by means of a front-panel potentiometer from 3.5 ns to 50 ns.

The minimum pulse pair separation of the Model 364 AL/365 AL is under 6 ns for an equivalent CW rate of greater than 160 MHz.

The Model 365 AL is a deadtimeless circuit and will respond to input signals even when an output is already present. The minimum pulse pair separation is under 6 ns for an equivalent CW rate of greater than 150 MHz. If a second coincidence is detected during the time the output from a first coincidence is being produced, the unit will extend the output duration to reflect the occurrence of the second signal. The net output pulse, being the logical sum of two standard output pulses, is of standard amplitude and retains the time information contained in the input signals.

The Model 364 AL/365 AL **offers** non-multiple-pulsing operation to assure unambiguous response to input pulses regardless of their amplitude or duration. The 364 AL/365 AL will not produce multiple pulses even with input pulses that substantially exceed the output pulse in duration.

SPECIFICATIONS

Number of Channels: Two, both identical.

Input Levels: NIM logic levels: logical 0, 0 mA \pm 2 mA; logical 1, 16 mA \pm 2 mA.

Input Impedance: 50 Ω \pm 5%; value of impedance is constant up to the limit of input protection for negative inputs.

Input Protection: \pm 5 volt protection for pulses. DC overload characteristics are determined by the 250 mW dissipation limit of the 50 Ω input terminating resistor.

Input Coupling: Direct; coupling is independent of input risetime, duration and rate.

Input Reflections: Dependent upon input risetime; less than 10% for input signal of 2 ns risetime or greater.

Gate: Logic unit may be inhibited by application of NIM Bin Gate. Bin Gate enters module via pin of rear multipin connector. Switch located on back panel disconnects Model 364 AL/365 AL from Bin Gate line. Clamping Bin Gate to ground from +5 volts inhibits. Clamping circuit must sink 3 mA per module. Bin Gate circuit is direct-coupled. Rise and fall times are \leq 50 ns for 365 AL and \leq 20 nsec for 364 AL.

Negative Outputs: Two, both with paralleled connectors driven by common high impedance current source. Quiescently, 0 mA, current source switches to -32 mA during output.

Positive Output: One, complimentary, paralleled connectors, quiescently -32 mA (-1.6V into 50 Ω load), switching to zero volts during an output.

Output Duration: Equal to time overlap of input signals or fixed 4.0 ns max., (3.5 ns typical) switch selected for Model 364 AL.

4 ns FWHM to 50 ns, continuously adjustable by means of front-panel width control for Model 365 AL.

Output Rise and Fall Times: 1.2 ns typical, 10% to 90%; fall time slightly longer on wider widths.

Output Duration Stability: Less than 0.1%/°C from 20°C to 60°C.

Coincidence Width: 1 ns up, determined by input pulse duration.

Double Pulse Resolution: Minimum separation to resolve two pulses is typically under 6 ns.

Maximum Rate: 160 MHz typical, input and output; defined for input signals of -600 mV, 3 ns FWHM.

Functions: ANDing, ORing, Majority, Inhibit and Complementary logic.
<20 ps rms.

Multiple Pulsing: None, one and only one output pulse is produced for each input pulse regardless of input pulse amplitude or duration.

Power Requirements: +12 volts at 115 mA, -12 volts at 150 mA, 120 VAC at 33 mA for Model 364 AL.

8.8 watts total; +12 volts at <120 mA, -12 volts at 165 mA, -24 volts at 22 mA, 120 VAC 33 mA; voltages must be regulated to $\pm 0.1\%$ for Model 365 AL.

Counting Efficiency: Deadtimeless operation; recovery time is less than output pulse duration; there is no deadtime following output pulse at output durations greater than 8 ns; output duration will update to reflect new input if retriggered while output pulse is present.
(Model 365 AL only)

Packaging: The Model 364 AL/365 AL are packaged in conformance with AEC standard for nuclear modules (AEC Report TID 20893 Rev.) Completely compatible physically and electrically with LRS Power Chassis Model 108P, and with any other AEC standard power bin of any manufacturer. Model 364 AL/365 AL is a single-width module using Lemo-type connectors and Model 364 AL/365 AL is a double-width module using BNC-type connectors.

CIRCUIT DESCRIPTION

The Model 364 AL Dual 4-Fold Logic Gate is composed of five basic sections as indicated on the block diagram: a current switch for each input, a set of selectable current sources to set coincidence level, a current summing buffer, a pulse OR ing section, and the output buffers. The Model 365 AL employs a tunnel-diode based trigger stage to provide standardized pulses to the timing stage.

The current switch at each input provides input buffering with proper termination and On-Off control, and causes an 8.6 mA current to be subtracted from the coincidence level current for the duration of the input pulse. The current switch is composed of a MC 1664 non-inverting AND gate. The input may be disabled by shorting the second input of the gate to ground causing the signal input to be ignored. Quiescently, the output of the 1664 gate is "high" (0 volts) and is supplying the current to the 523 Ω resistor which serves as the 8.6 mA current source. An input signal level (\sim 600 mV or greater) causes the open emitter of the output of the 1664 gate to go low, allowing the MBD-101 diode to conduct the 8.6 mA. Since the anodes of the four MBD-101's are connected as a current summing point, each input signal causes 8.6 mA to be subtracted from the coincidence level current source.

The coincidence level current source supplies from 14.3 mA to 40.1 mA depending upon the coincidence level selected. In the "singles" position, the current source supplies 10 mA for the current source buffer, plus 4.3 mA, or 1/2 of an input current switch unit. Each additional level selected over a singles requirement increases the available current by 8.6 mA. The amount of a current available is supplied by the collectors of two transistors connected in a Darlington configuration. The emitters are held at a constant voltage equal to the reference voltage generated by the coincidence level selector. The actual current is determined by the voltage across the two paralleled 432 Ω resistors at the transistor emitters. Any difference between the emitter voltage and the reference voltage is detected by the 741 operational amplifier which adjusts the Darlington input to provide the correct output. This circuit provides stable currents independent of temperature and transistor characteristics.

The current summing buffer section of the 364 AL provides the impedance matching and level shifting required to drive both an inverter and the OR ing stage. It is composed of an emitter follower to decouple the MC1660 input capacitance from the summing point, a 47 Ω resistor to provide the proper DC level, and several current source resistors to provide proper current biasing. The emitter follower directly drives the OR ing section, and drives a MC 1660 inverter.

The inverter can be turned off by switching the front panel switch to Overlap. When switched to Clipped, the inverter supplies a complemented pulse with 1.5 ns inherent delay, which is further delayed by a 2 ns printed circuit delay line which is also supplied to the OR ing section.

The OR ing section of the 364 AL is used to drive the output stage or to completely inhibit the output signals if either veto or bin gate signals are present. The overlap of the normal and delayed complementary signals cause the 1660 gate to provide a clipped, 3.5 ns wide pulse which is independent of the duration of input signal overlap as long as the overlap is greater than 3.5 ns. If either a veto input signal or a bin gate level is present during the overlap, the 1660 will ignore the overlap and no output will be generated. (In Clipped mode, the veto or bin gate need only be present during the first 3.5 ns.) Both the veto input and the bin gate input use MC 1010 NAND gates as inverter/buffers. The outputs of these gates use source terminated printed circuit busses to provide fast, reflection-free connections from the MC 1010 outputs to the MC 1660 inputs.

The tunnel diode section of the 365 AL provides a fast-rise, fixed amplitude pulse anytime the inputs equal or exceed the coincidence level selected. Quiescently, the tunnel diode is in its low voltage state, being supplied with approximately 8.4 mA from the 510 Ω resistor to the -5 volt supply. When the current from the input current switch exceeds that which is available from coincidence level current source, the voltage at the current summing junction drops. This is transmitted through the differential stage (Q3, Q4) to the 10 mA tunnel diode, causing the tunnel diode to switch to its high voltage state. This in turn allows I.C. AB pin 14 to switch to its positive state. This transition is passed onto the next section of I.C. AB through the 43 ohm resistor, in addition to driving a 2 ns printed circuit delay line. After the 2 nsec delay the emitter of Q5 is switched from approximately -1.5 volts to -.8 V thereby back biasing the FD777 diode allowing the current in the tunnel diode to drop to a level just sufficient to keep the diode in its high voltage state. When the input coincidence condition is removed the differential stage switches back to its quiescent state and allows the T.D. to switch back to its low level state.

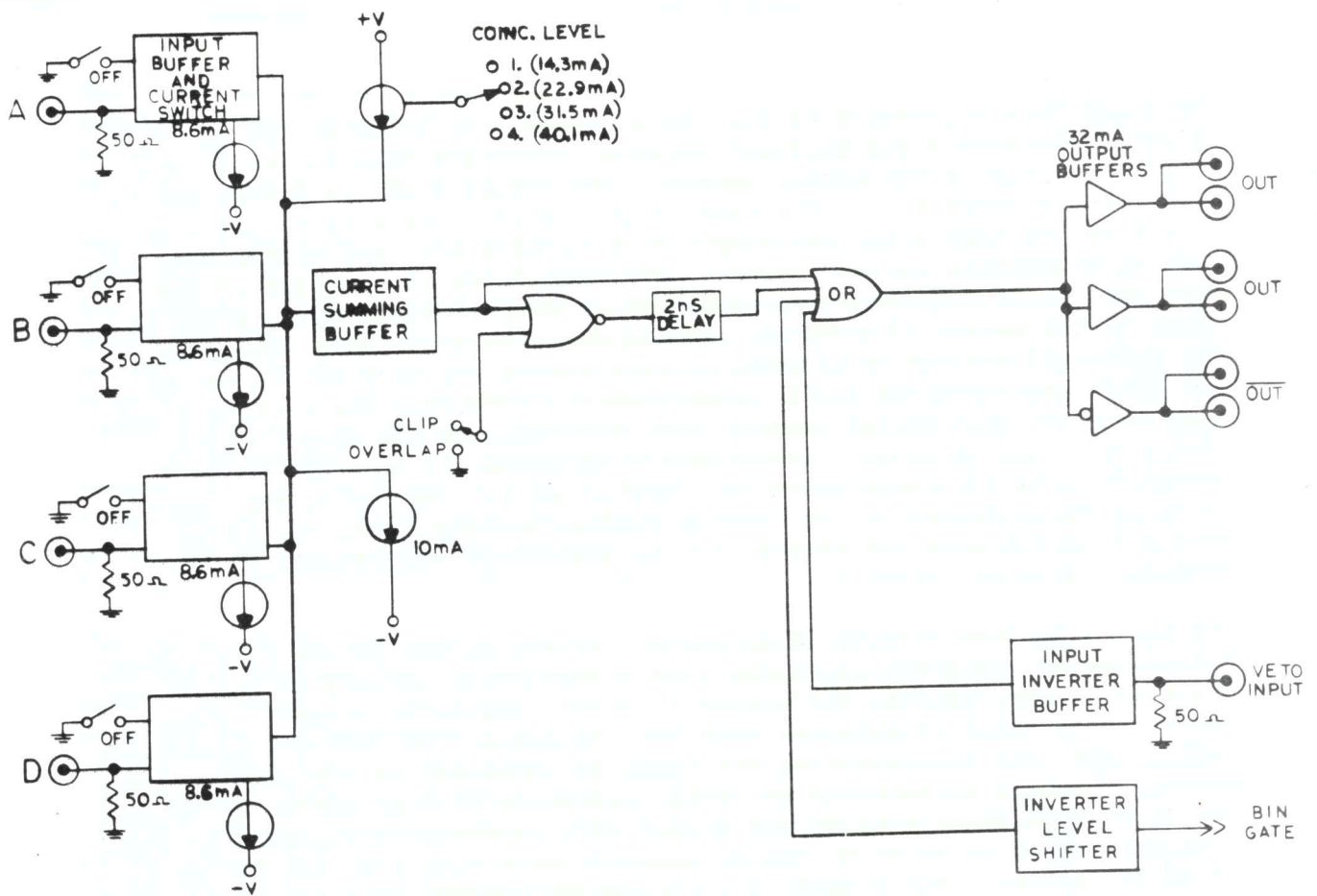
The output of the delay line also drives one input of the veto gate I.C. AB (pins 12, 13 & 15), which provides a delayed signal at its output. The overlap of the normal and delayed signals cause I.C. AB-3 to provide a 2 nsec wide current pulse which is independent of the duration of input signal overlap. If either a veto input signal or a bin gate level is present during the 2 nsec overlap the overlap will be ignored and no output will be generated. The 2 nsec current pulse is supplied to the pulse forming section which generates the desired width output pulse.

The pulse-forming section of the 365 AL, each time a current pulse is received, generates a standardized pulse with a width that is set by the front-panel 2 K Ω width potentiometer. The actual width is determined by a ramp and a comparator. The ramp is generated by raising a capacitor to a fixed voltage using the output of I.C. AB pin 3, and discharging it with an adjustable current source. The comparator is composed of the last section of I.C. AB which generates an output signal whose width is equal to the amount of time the ramp is above an adjustable threshold. The threshold and the adjustable current source are both determined by the front-panel-mounted width potentiometer. Coupling the threshold and ramp slope in this manner permits stable control of the output width over a 4.0 - 50 ns range. Deadtimeless operation is inherent in this design because anytime a pulse is received at I.C. AB pin 3, the capacitor is again raised to the initial rundown voltage. The resulting output thus reflects the receipt of the additional coincidence by extending the output width.

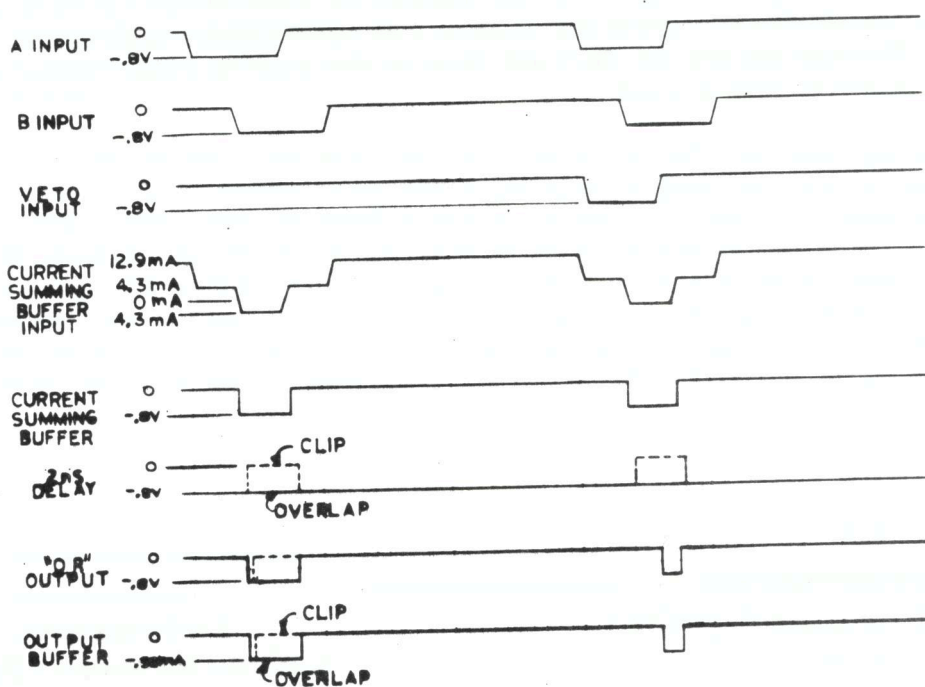
The output buffers provide 32 mA current source output pulses with widths determined by the previous stage. The differential outputs of the OR ing stage drive two separate differential current switching stages. Quiescently, each stage is balanced with one transistor "on" and one transistor "off". The "on" transistor of one stage is connected to the complementary output, which is quiescently at 32 mA, switching to 0 mA during an output. The "off" transistors tied to the normal (OUT) connectors quiescently supply 0 mA and switch to 32 mA during an output. Each output drives two parallel connectors. All outputs are limited by the MBD 101 clamp diodes, and the -1.5 volt supply (Q9 & Q10) 0, to -2 volts.

In addition to using the standard +12 volts from the power connector, the Model 364 AL/365 AL also requires +0.8 and -5.0 volts. This is supplied by an internal 5.8 volt supply using 120 VAC from the rear power connector. The positive side of the supply is referenced to +0.8 volts by an emitter follower operating from a 741 operational amplifier. The reference for the op-amp is derived from a resistor divider connected between +12 volts and ground.

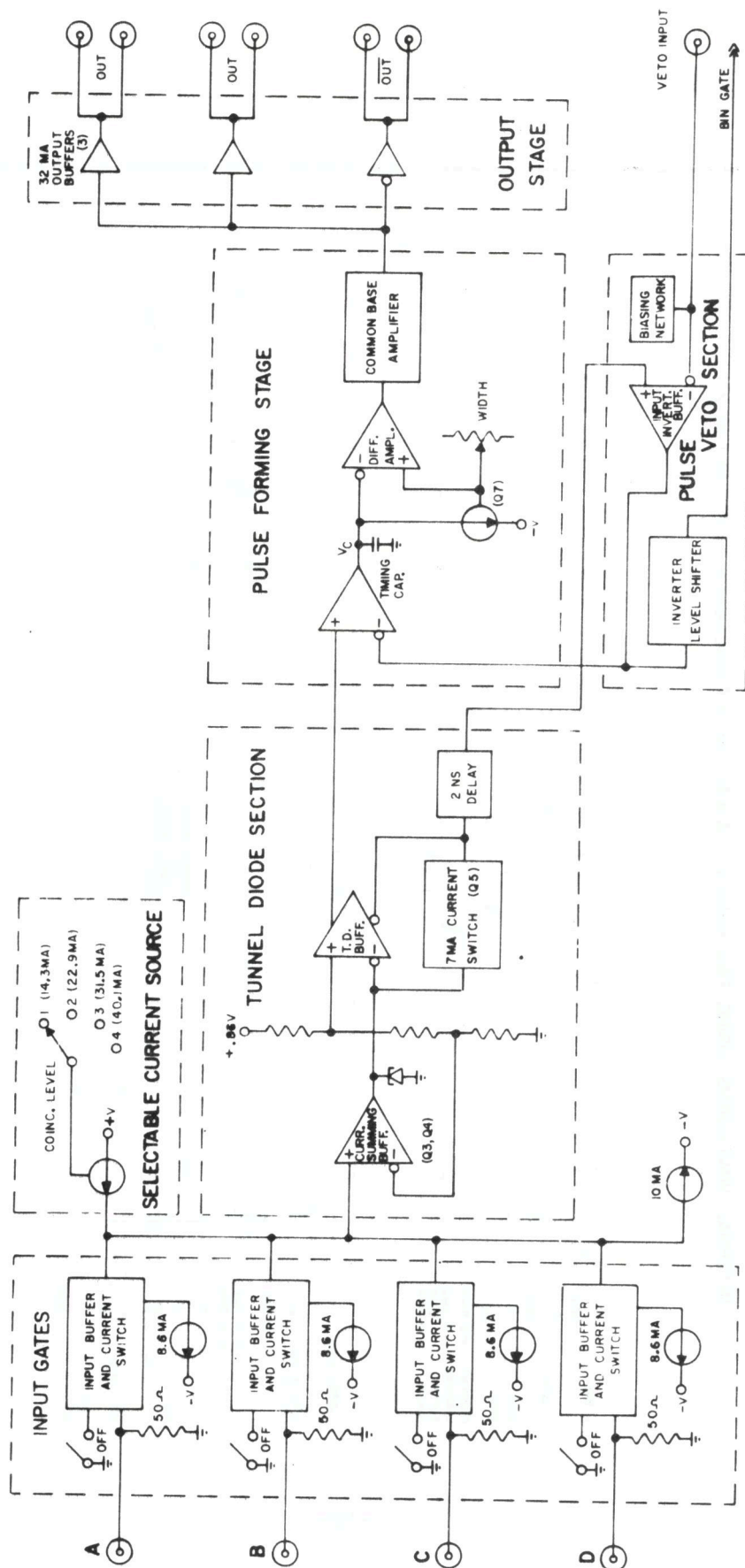
MODEL 364 BLOCK DIAGRAM



INTERNAL WAVEFORMS USING TWO INPUTS - A & B
WITH COINCIDENCE LEVEL SET AT 2



MODEL 365 BLOCK DIAGRAM



INTERNAL WAVEFORMS USING TWO INPUTS - A & B, WITH COINCIDENCE LEVEL SET AT 2.

