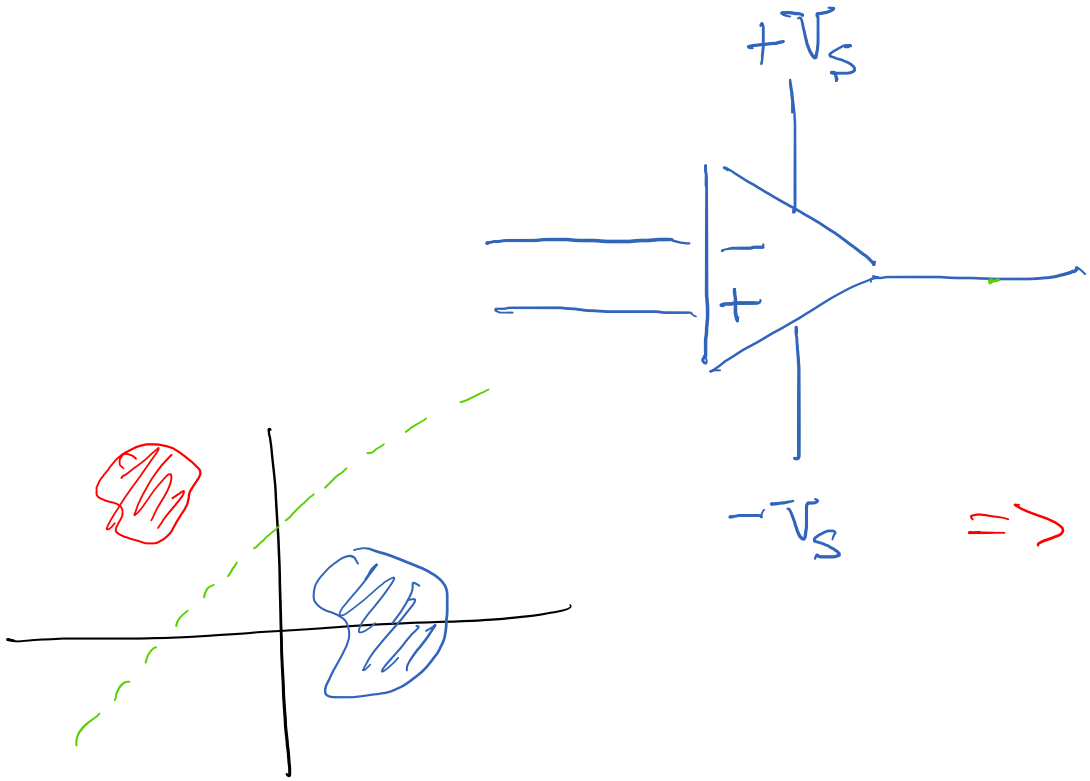
COMPARATOR / LATCH



$$V_{out} = A[V_+ - V_-]$$

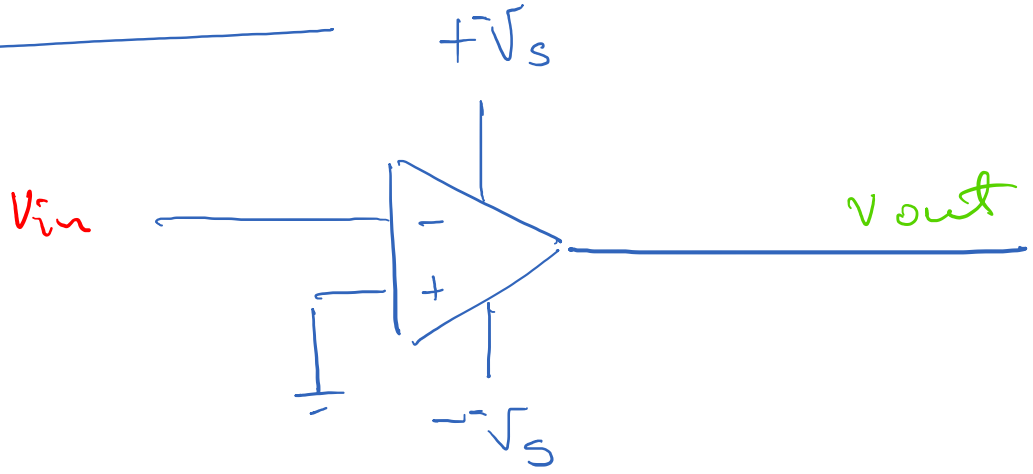
$$A \gg 1$$

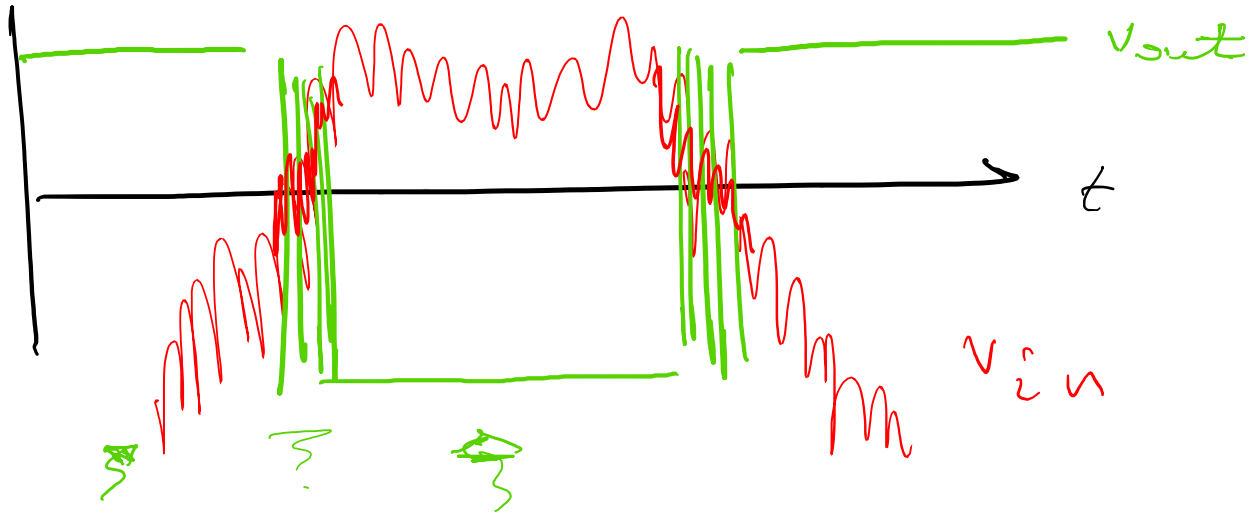
$\Rightarrow$ output either @

$+V_S$ [For $V_+ > V_-$]

$-V_S$ [For $V_+ < V_-$]

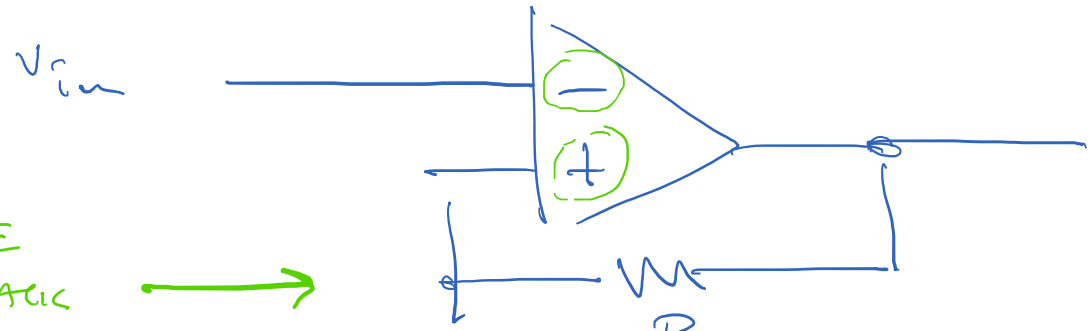
NAIVE APPROACH.





BETTER APPROACH

LOOKS LIKE NONINVERTING AMP.



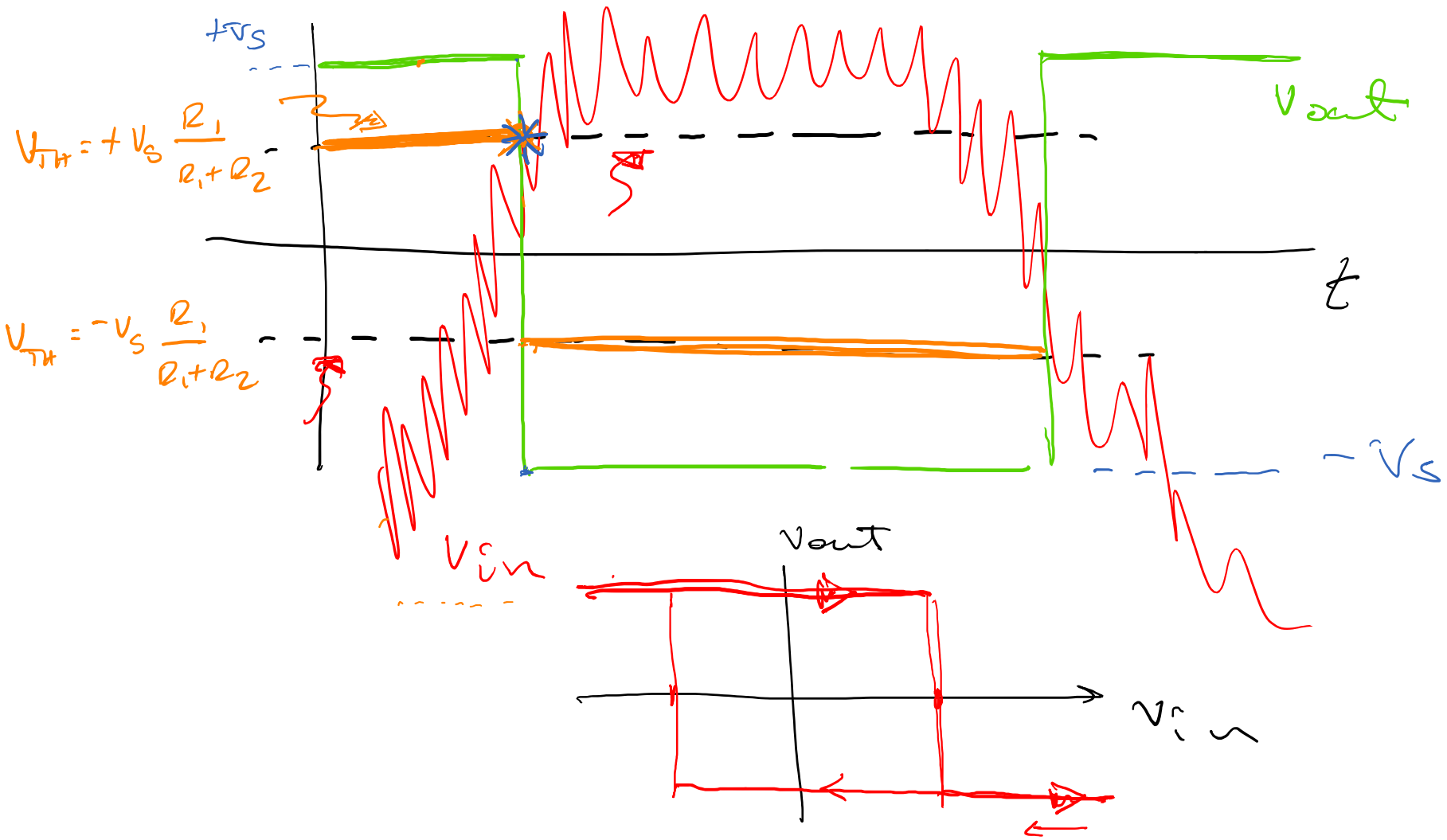
POSITIVE FEEDBACK TO ESTABLISH HYSTERESIS IN THRESH. DETECTOR.

HERE $V_- \neq V_+$

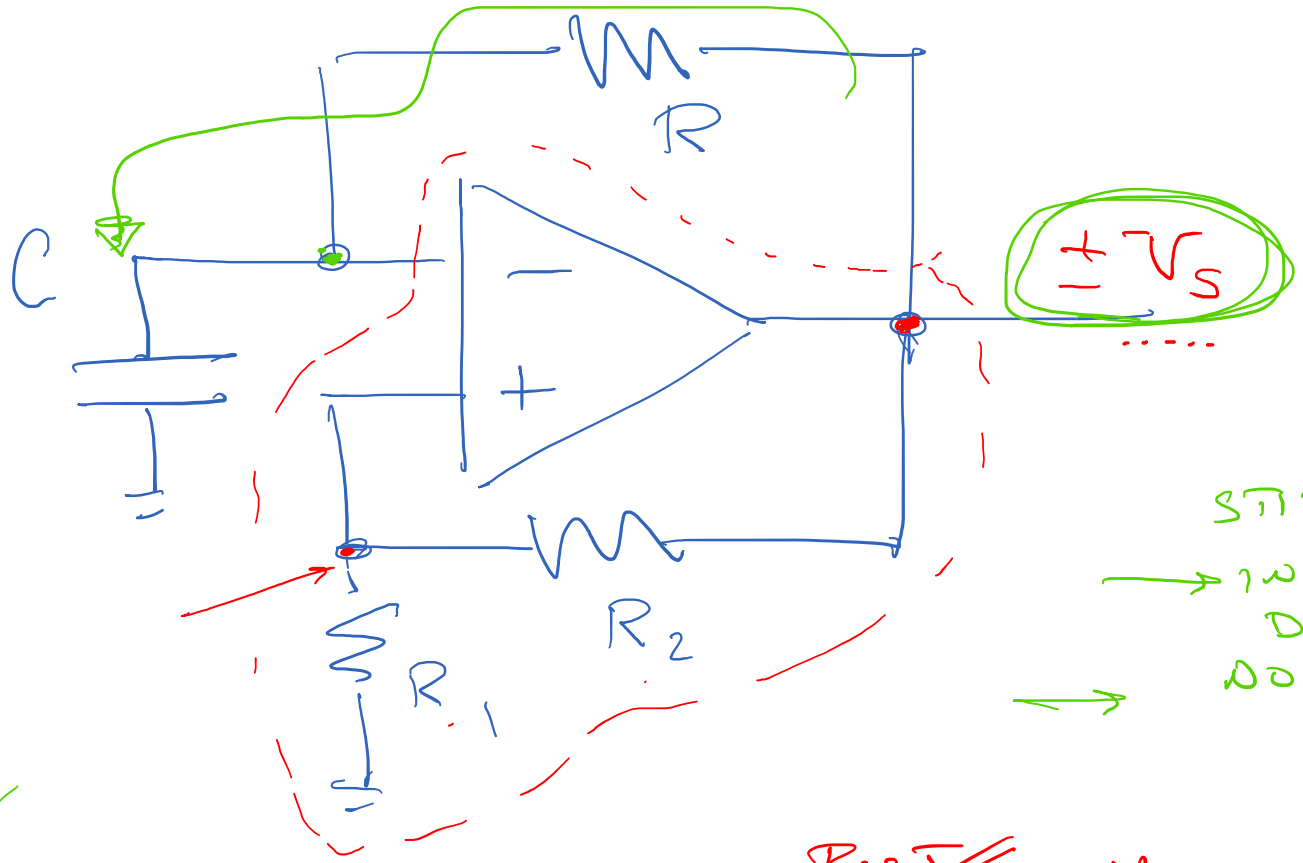
BUT. STILL, INPUTS DRAW NO CURRENT.

$$V_{TH} = \pm V_S \cdot \frac{R_1}{R_1 + R_2}$$

$V_{TH} = V_+$


+Vs
$V_{TH} = +V_S \frac{R_1}{R_1+R_2}$
$V_{TH} = -V_S \frac{R_1}{R_1+R_2}$
Vout
t
-Vs
Vin
Vout
Vin

RELAXATION OSCILLATOR



OLD FAITHFUL

STILL TRUE

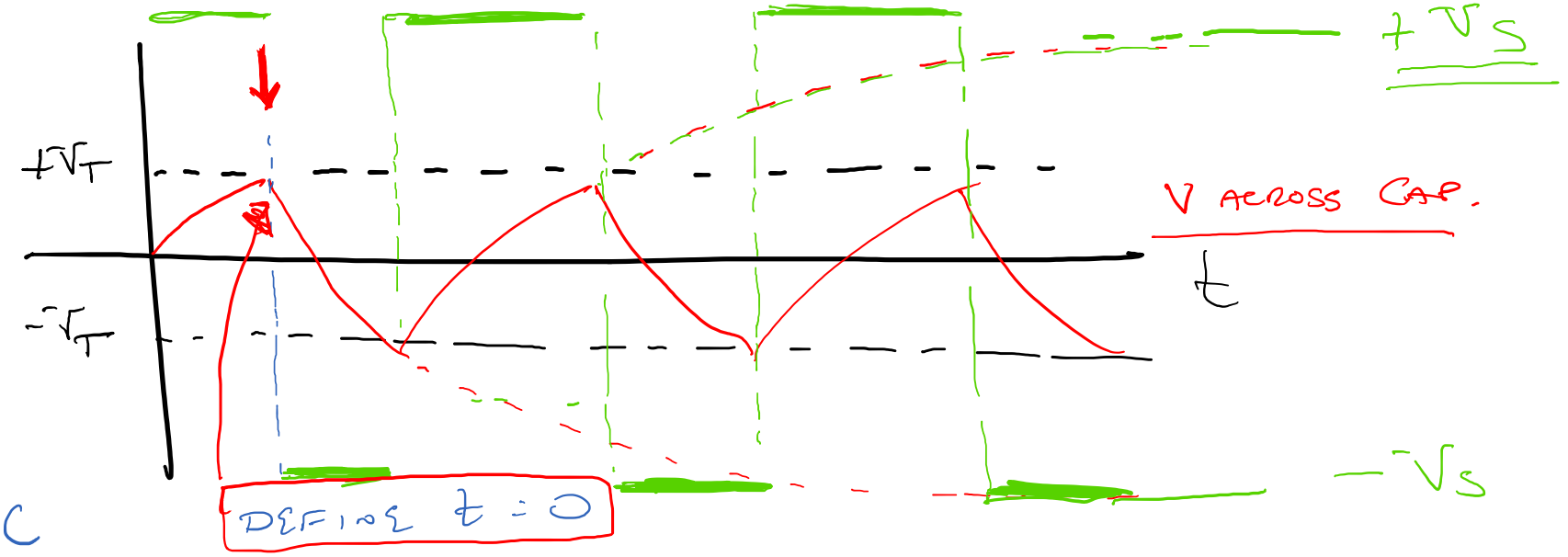
→ INPUTS DRAW NO [NEGLIGIBLE] CURRENT

→

BUT

→

$V_+ \neq V_-$



$\tau = RC$

$\Rightarrow V_{CAP}(t) = A e^{-t/\tau} + B$; $V_{CAP}(t=0) = +V_T$

$V_{CAP}(t \to \infty) = -V_S$

$\Rightarrow V_{CAP}(t) = (V_T + V_S) e^{-t/\tau} - V_S$

PERIOD ?

$$V_T = V_S \frac{R_1}{R_1 + R_2}$$

PERIOD T

$$-V_T = (V_T + V_S)\, e^{-\frac{T}{2\tau}} - V_S$$

$$\Rightarrow T = 2\tau \ln\left(\frac{V_S + V_T}{V_S - V_T}\right)$$

e.g. $V_T = V_S/2 \Rightarrow T = 2\tau \ln 3$

$R_1 = R_2$

BOOLEAN ALGEBRA

LOGICAL 0 & 1 ["FALSE" & "TRUE"]

BITS A AND B

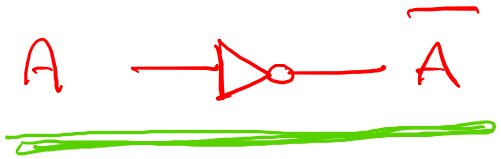
SINGLE BIT OPERATION

NOT A $\quad \bar{A}$

TRUTH TABLE

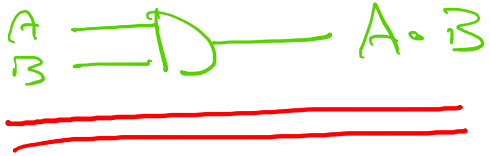
INPUTS → A | $\bar{A}$ ← OUTPUTS

A	$\bar{A}$
0	1
1	0



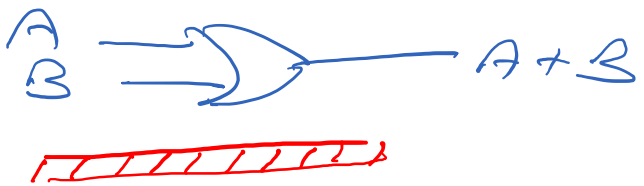
TWO-BIT OPERATIONS

A AND B $A \cdot B$



A	B	A·B
0	0	0
0	1	0
1	0	0
1	1	1

A OR B $A + B$



A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOR 

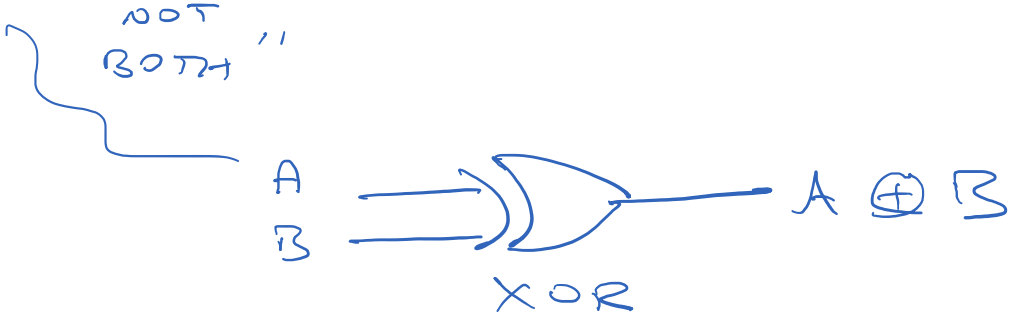
NAND 

→ EXCLUSIVE OR [XOR]

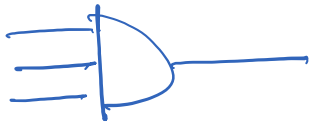
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

"A OR B BUT NOT BOTH"

A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0



3-BIT OPERATIONS

e.g. 3-BIT AND  ETC.

THEOREMS OF BOOLEAN ALGEBRA

- $A + 1 = 1$
- $A + 0 = A$
- $A \cdot 1 = A$
- $A \cdot 0 = 0$
- $A + A = A$
- $A \cdot A = A$
- $A + \bar{A} = 1$
- $A \cdot \bar{A} = 0$

DISTRIBUTION

$$A \cdot (B + C) = AB + AC$$

COMMUTATION

$$A + B = B + A$$

$$AB = BA$$

EXAMPLES

$$A + BC = (A + B)(A + C)$$

$A + BC = A \cdot 1 + BC$

$= A \cdot (1 + B) + BC$

$= A \cdot 1 + AB + BC$

$= A \cdot (1 + C) + B(A + C)$

$= A \cdot (A + C) + B(A + C)$

$= (A + B)(A + C)$

$A \cdot 1 = A \cdot A$

[DISTRIBUTION]

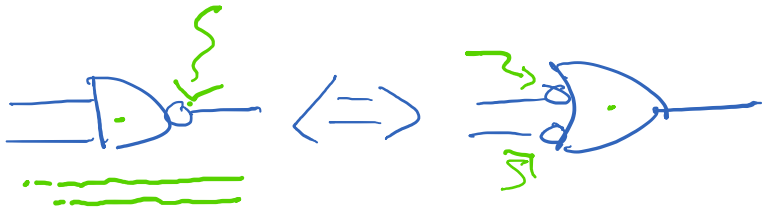
De Morgan's Theorem

I. $\overline{A \cdot B} = \overline{A} + \overline{B}$

NOT (A AND B) = NOT A OR NOT B

II. $\overline{A + B} = \overline{A}\,\overline{B}$

NOT (A OR B) = NOT A AND NOT B

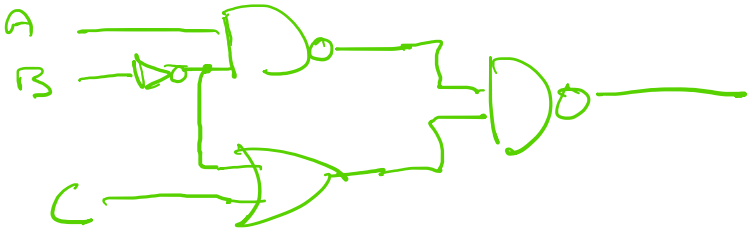


eg

A	B	$\overline{AB}$	$\overline{A} + \overline{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

EXAMPLE

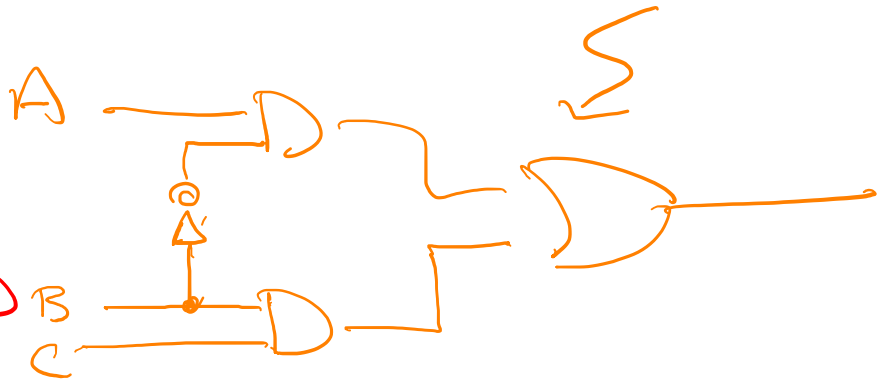
$$\overline{(A\cdot\overline{B})\cdot(\overline{B}+C)}$$



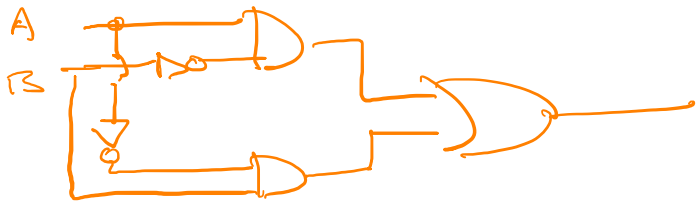
$$= A\overline{B} + \overline{(\overline{B}+C)}$$

$$= A\overline{B} + B\overline{C}$$

ANOTHER : XOR FROM NAND



$$A\cdot\overline{B} + \overline{A}\cdot B$$

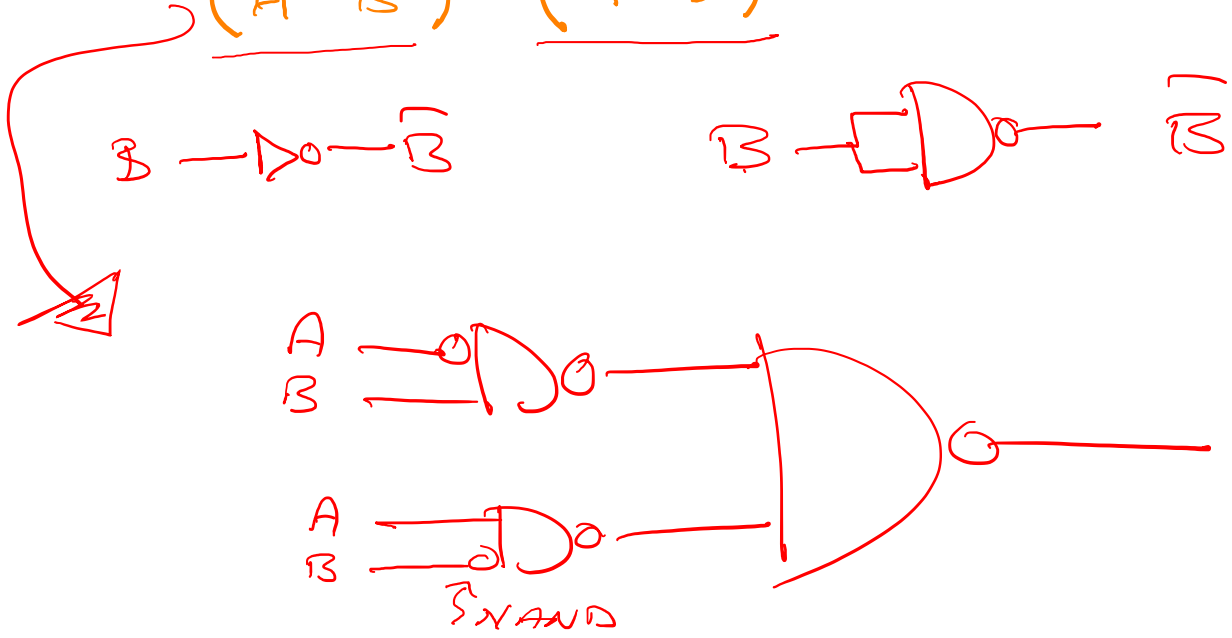


XOR

$$A \cdot \bar{B} + \bar{A} \cdot B$$

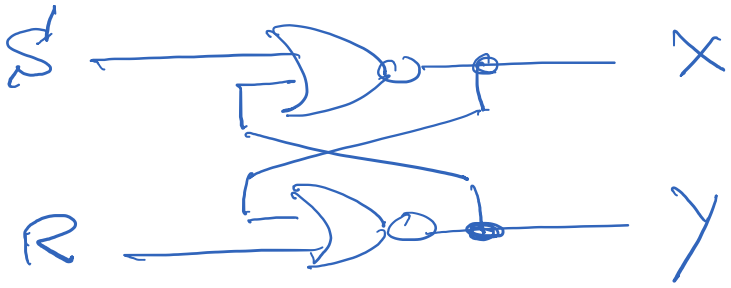
$$= \overline{A \cdot \bar{B} + \bar{A} \cdot B}$$

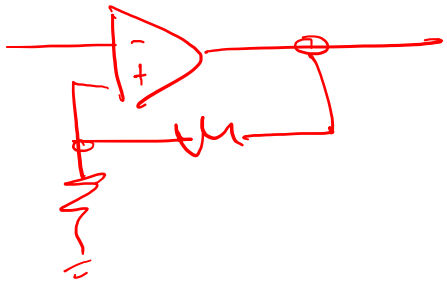
$$= \overline{(A \cdot \bar{B})} \cdot \overline{(\bar{A} \cdot B)}$$



DIGITAL LATCH

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0





TRUTH TABLE

INPUTS XY

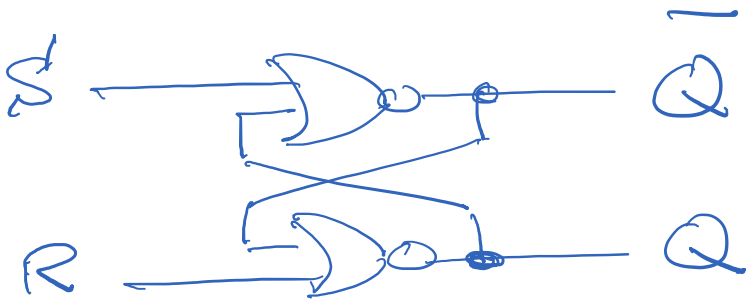
SR	00	01	10	11
→ 00	11	01	10	00
→ 01	10	00	10	00
10	01	01	00	00
11	00	00	00	00

(NOT USED)

→ MEMORY

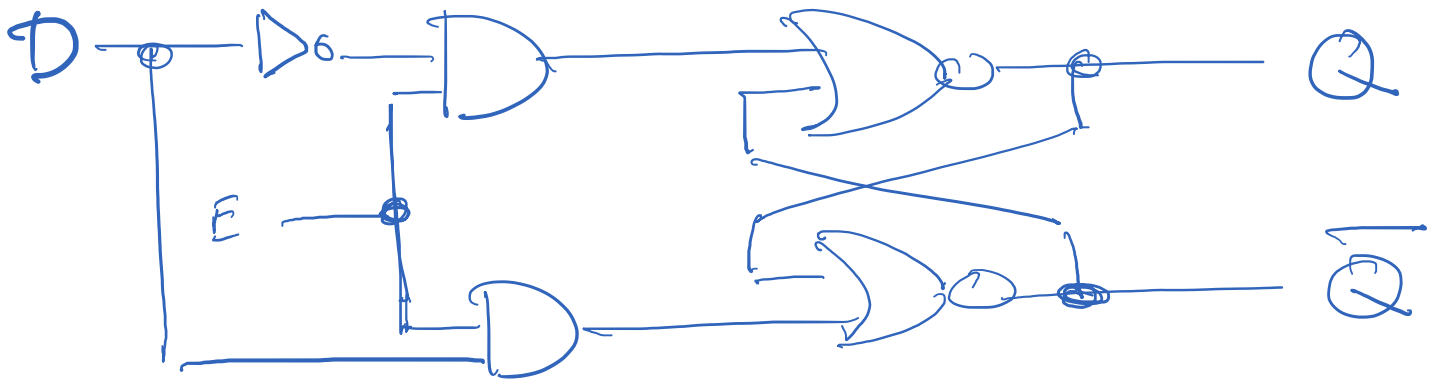
→ OUTPUT BITS XY

RESULTS TRUTH TABLE

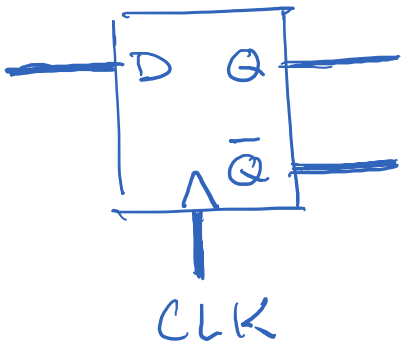


S	R	Q_{NEXT}
0	0	Q
0	1	0
1	0	1
1	1	X

GATED D-LATCH



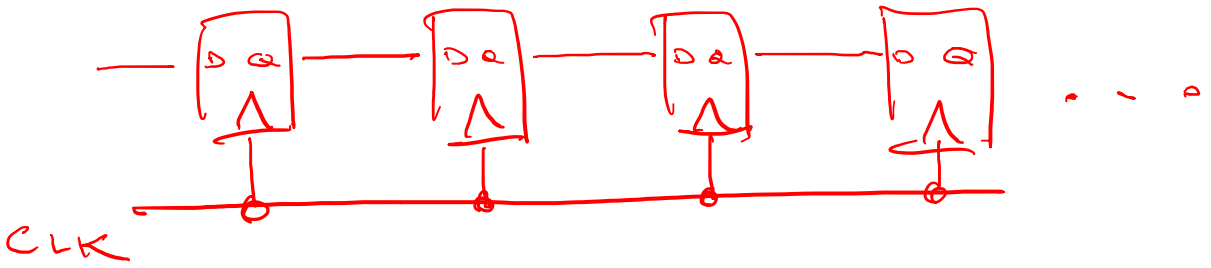
D FLIP FLOP



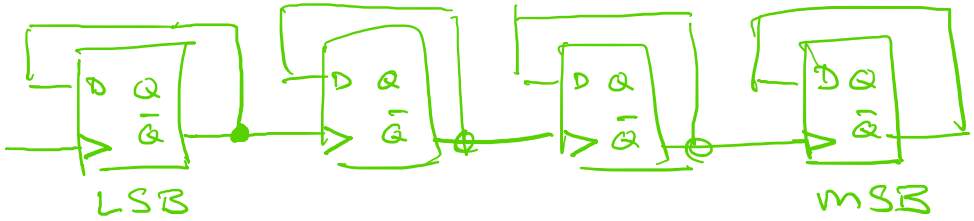
CLK	D	Q
RISING EDGE	0	0
RISING EDGE	1	1
NON RISING	X	Q

$Q_{next} = D$

SHIFT REGISTER



ASYNCHRONOUS COUNTER



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1