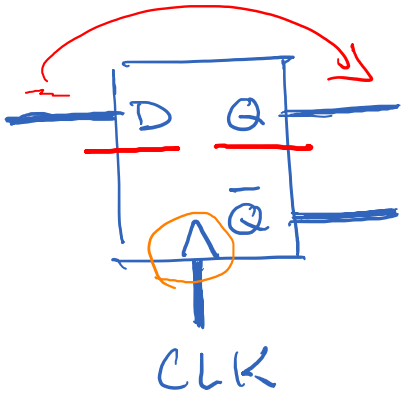
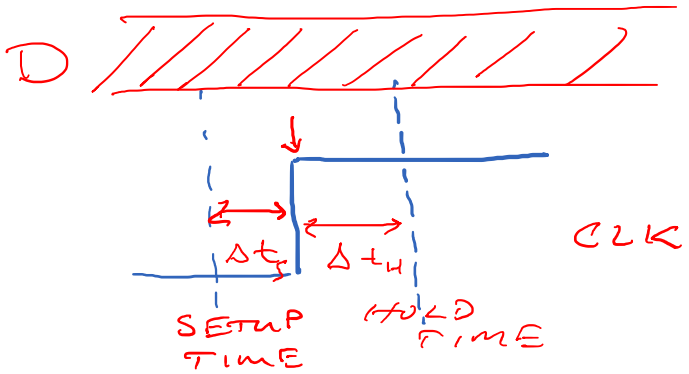
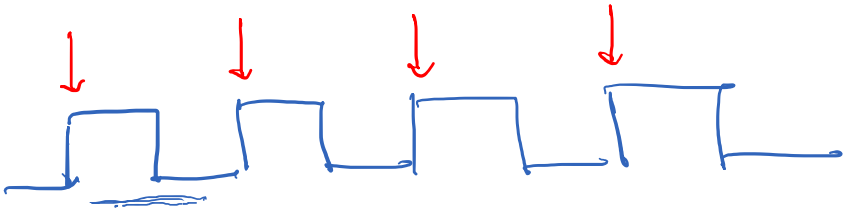
D FLIP FLOP





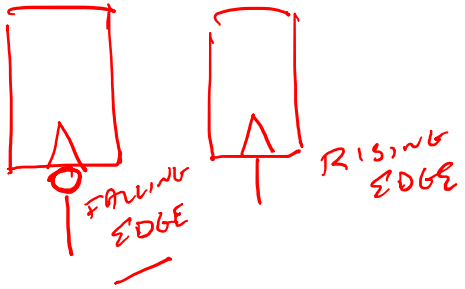


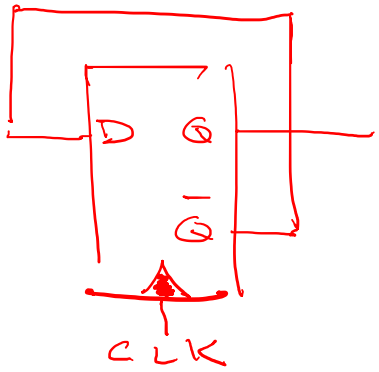
CLK	D	Q
RISING EDGE	0	0
RISING EDGE	1	1
NON RISING	X	Q

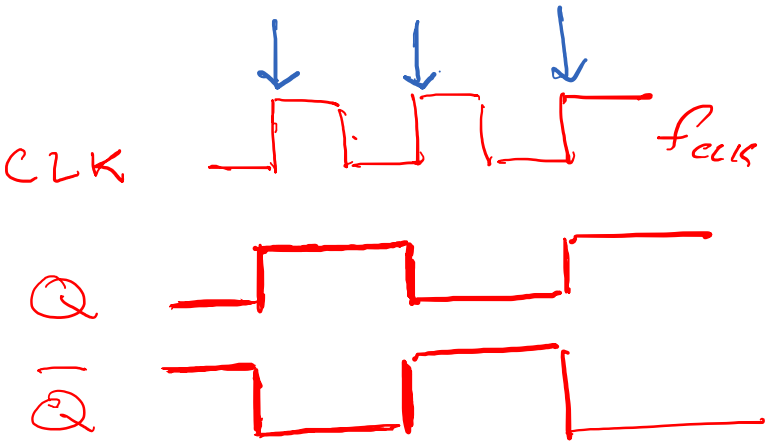
$Q_{next} = D$

$Q_{n+1} = D_n$

DIVIDE-BY-TWO



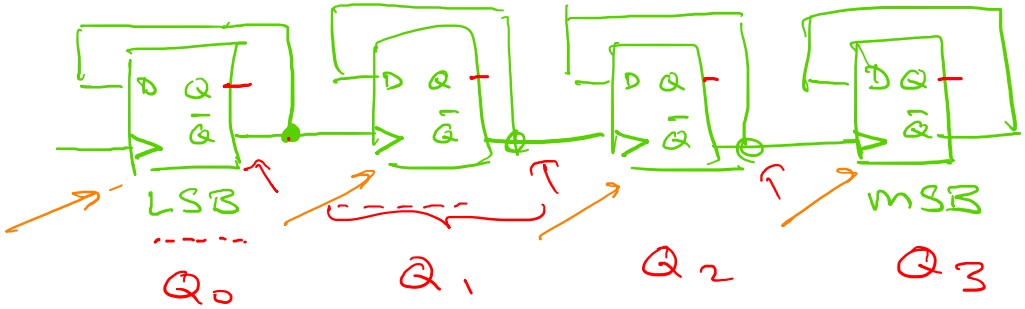


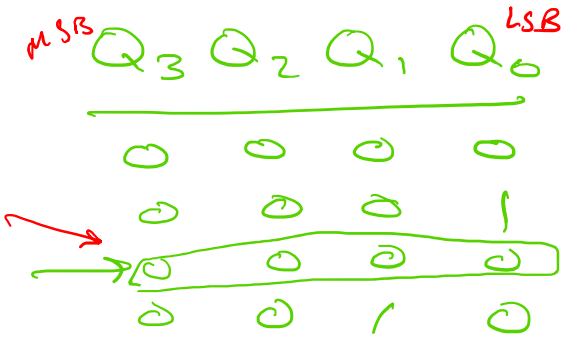


$f_{out} = \frac{1}{2} f_{CLK}$

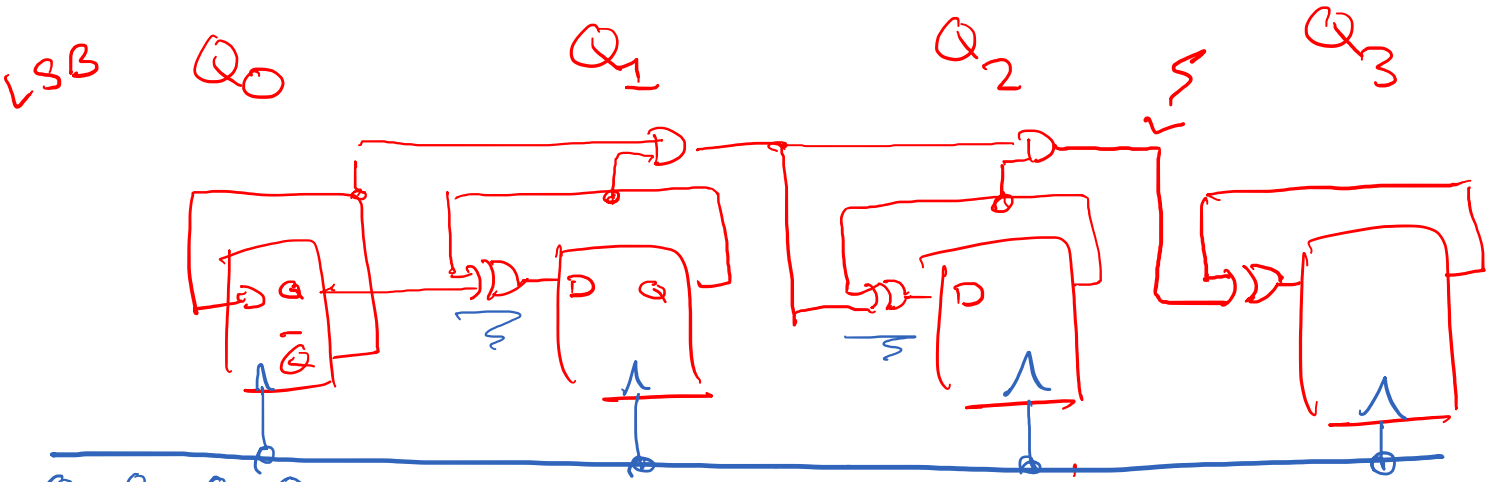
ASYNCHRONOUS COUNTER ←

"RIPPLE" COUNTER





SYNCHRONOUS COUNTER

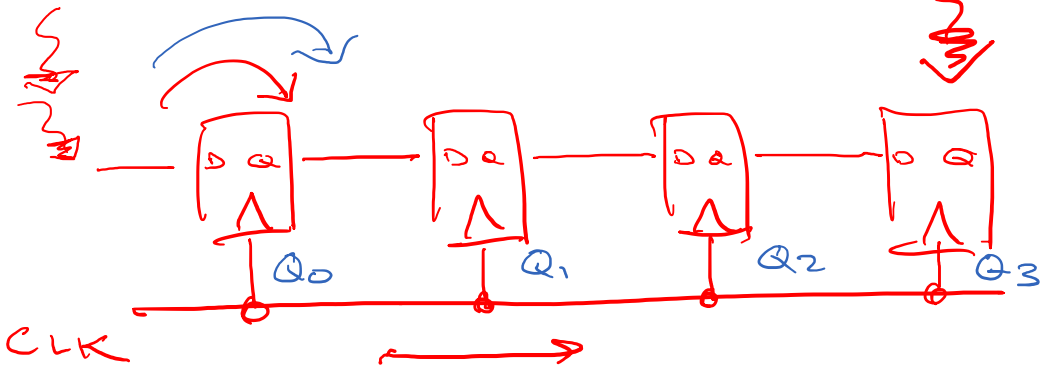


Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1

$$Q_{1,next} = Q_{0,prev} \oplus Q_{1,prev}$$

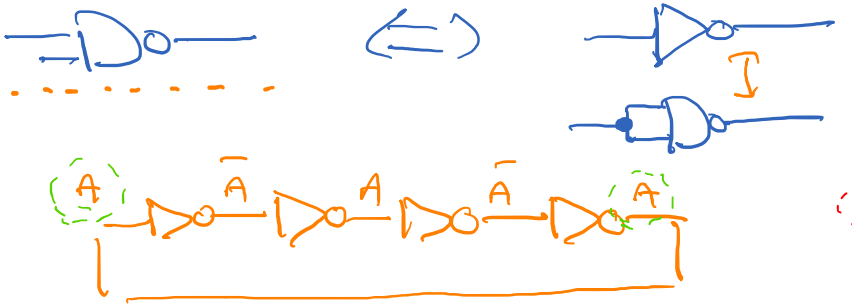
$$Q_{2,next} = (Q_{0,p} \cdot Q_{1,prev}) \oplus Q_{2,prev}$$

SHIFT REGISTER



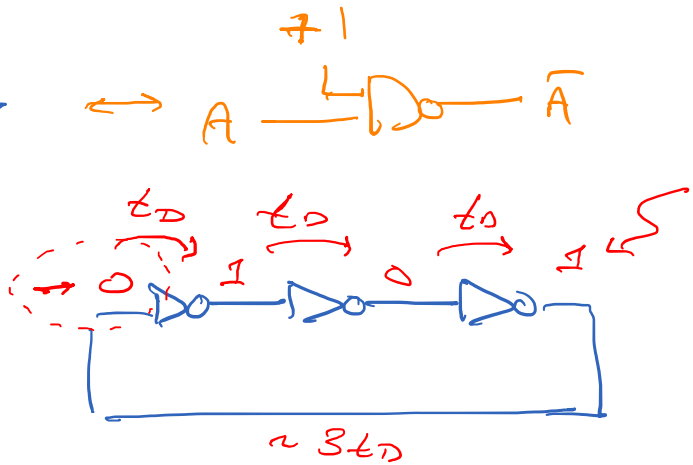
Q_3	Q_2	Q_1	Q_0	D
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	1	0	1	1
1	0	1	1	

RING OSCILLATOR



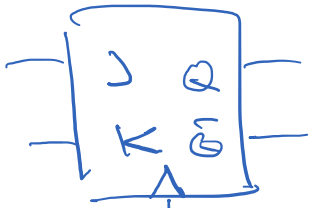
n ODD.

t



A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

J K. FLIP FLOP



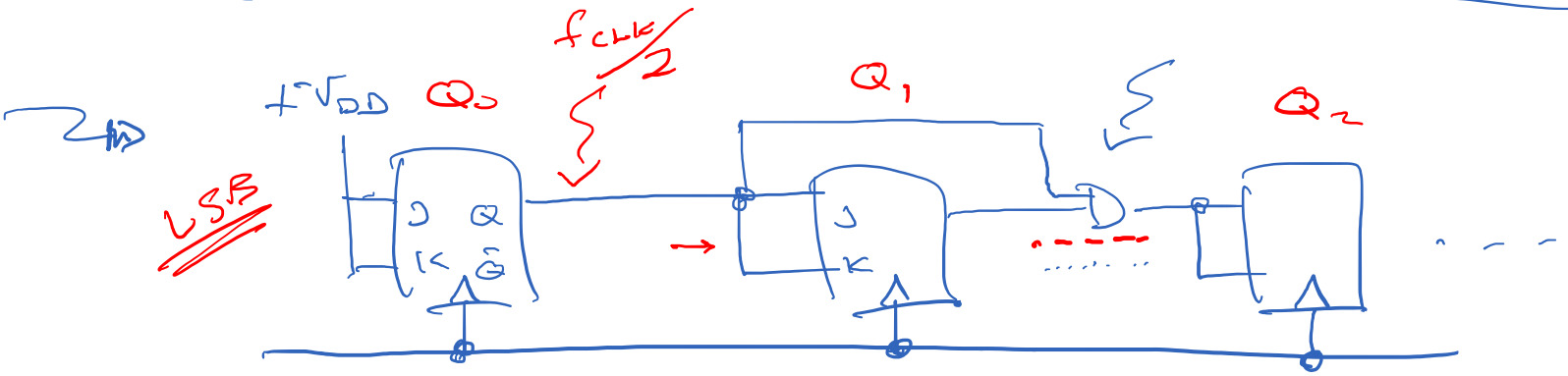
EDGE-TRIGGERED

J	K	Q_{next}
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

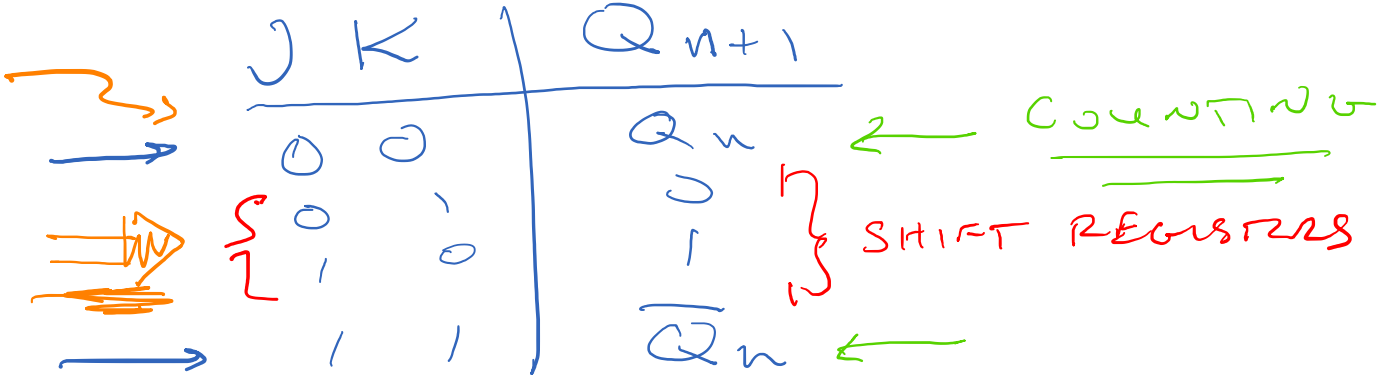
TOGGLE

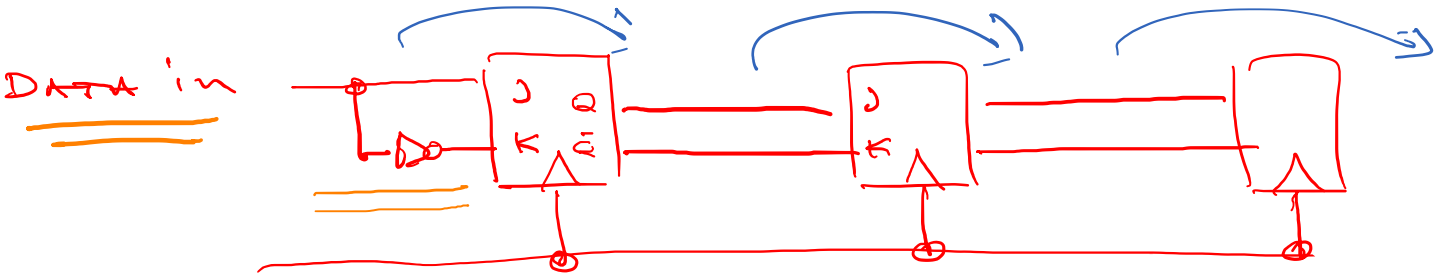
@ RISING EDGE

SYNCHRONOUS COUNTER



SHIFT REGISTER





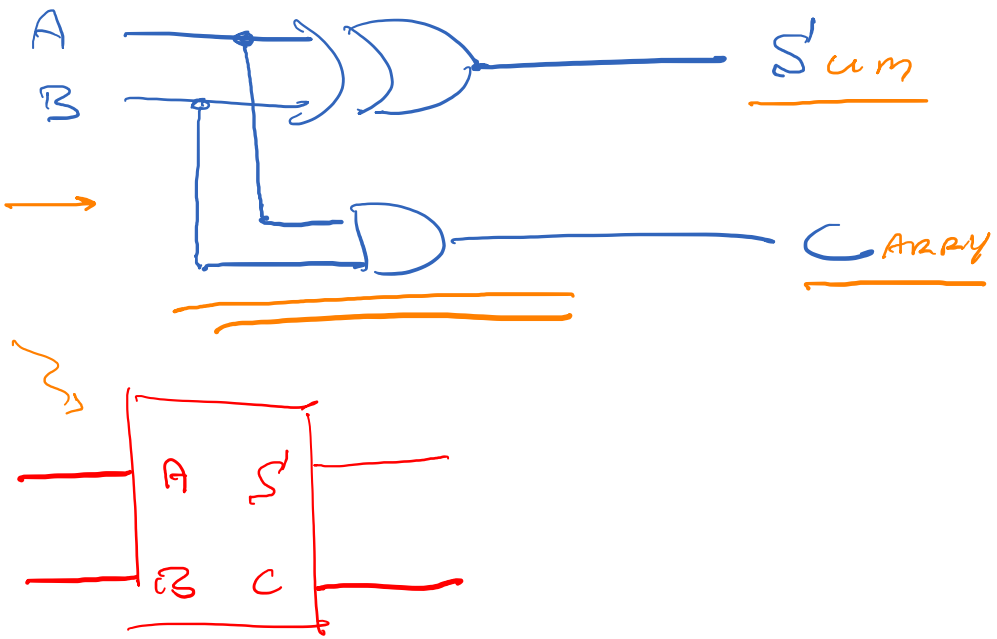
BINARY ARITHMETIC

HALF-ADDER

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

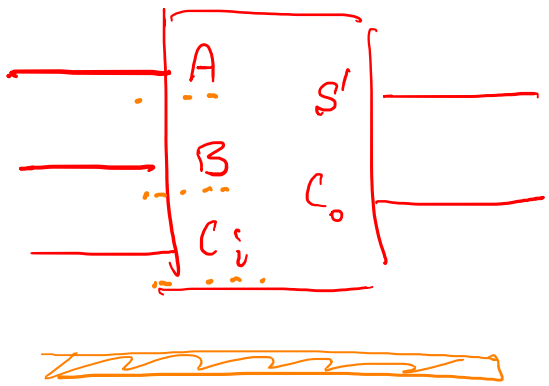
$S = A \oplus B$

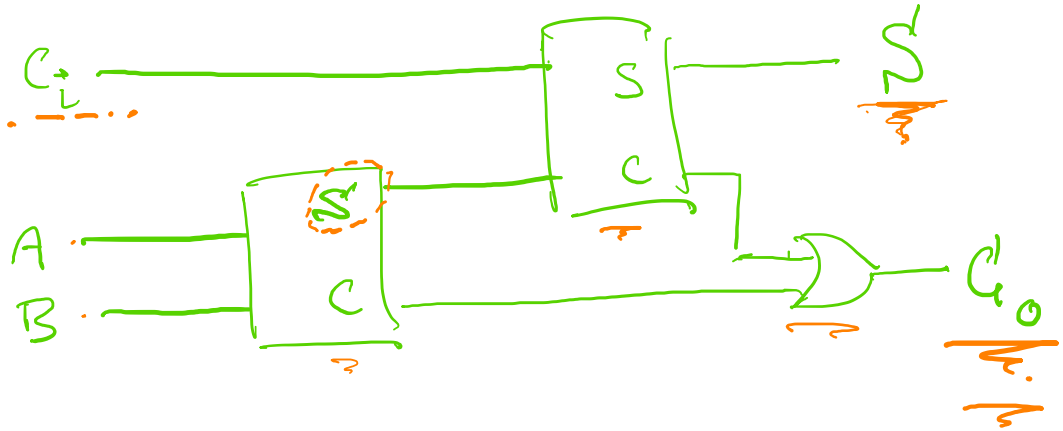
$C = AB$



FULL ADDER

A	B	C_i	S'	C_o
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1



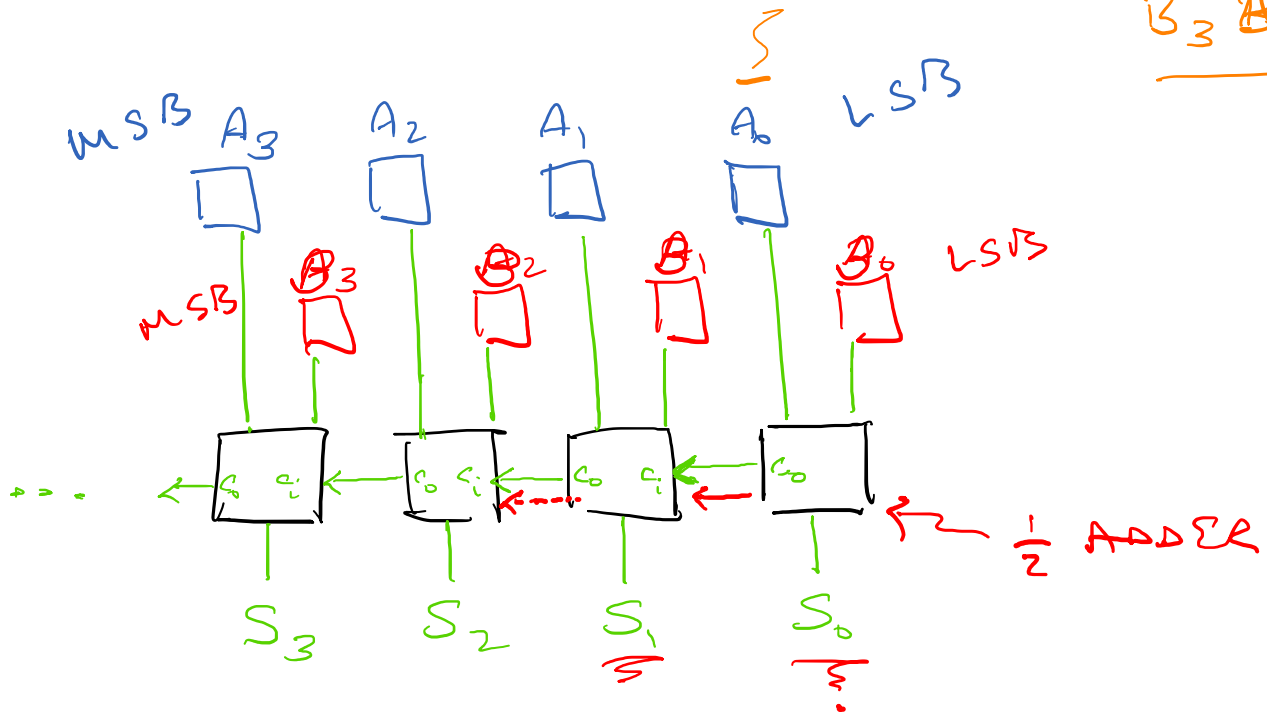


BINARY ADDITION

$A_3 A_2 A_1 A_0$

$B_3 B_2 B_1 B_0$

```
 1 1 1 1      7
+1 0 0 1      9
-----------
1 0 0 0 0    16
```



NEGATIVE NUMBERS

2's COMPLEMENT : FLIP ALL BITS & ADD 1

d	b
0	0 0 0
1	0 0 1
2	0 1 0
3	0 1 1
-1	1 1 1
-2	1 1 0
-3	1 0 1
-4	1 0 0

e.g. 2 − 3 :

```
  0 1 0
+ 1 0 1
-------
  1 1 1   => -1
```

−1 − 3

```
  1 1 1
+ 1 0 1
-------
1 1 0 0   => -4
```

3 → −3

3 : 0 1 1

STEP 1 : 1 0 0

STEP 2 : 1 0 1 → BINARY REP. OF −3

MULTIPLICATION

$3 \times 5 \overset{?}{=} 15$

eg

UNSIGNED

```
    0 1 1
    1 0 1
  -------
    0 1 1
  0 0 0
0 1 1
-------
0 1 1 1 1
```

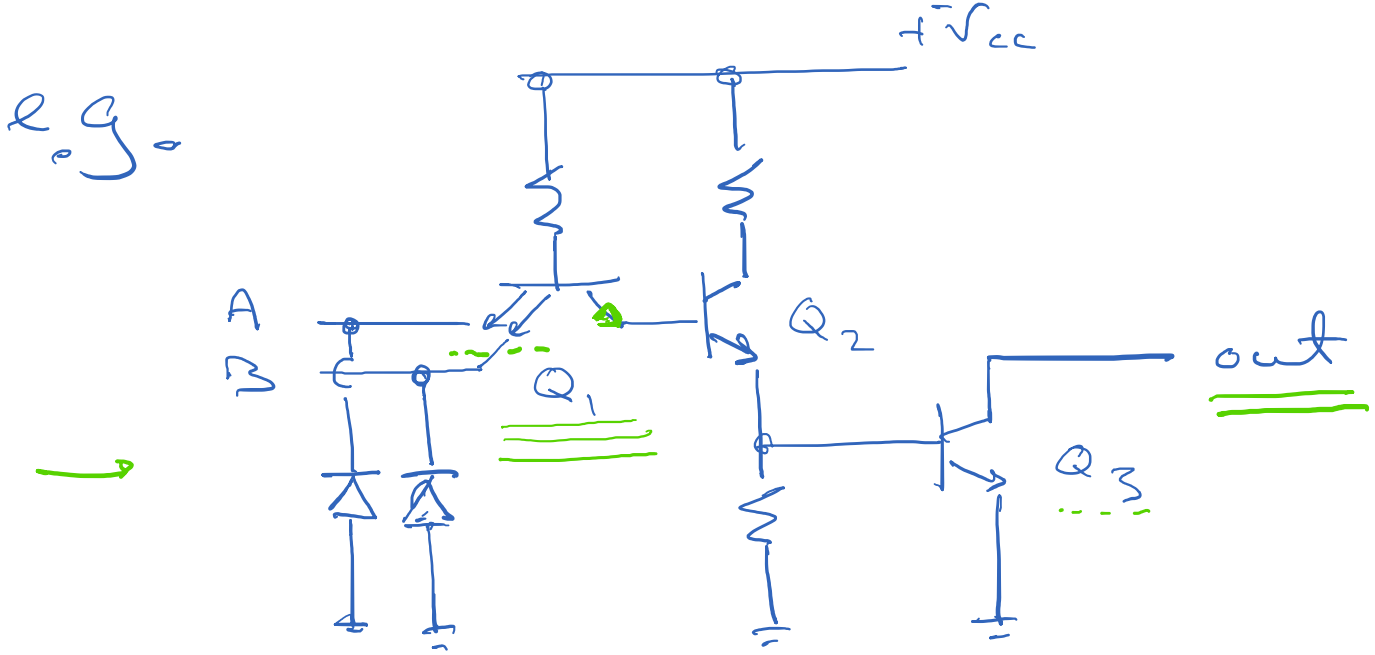
DIVISION

$15 \div 3 = 5$

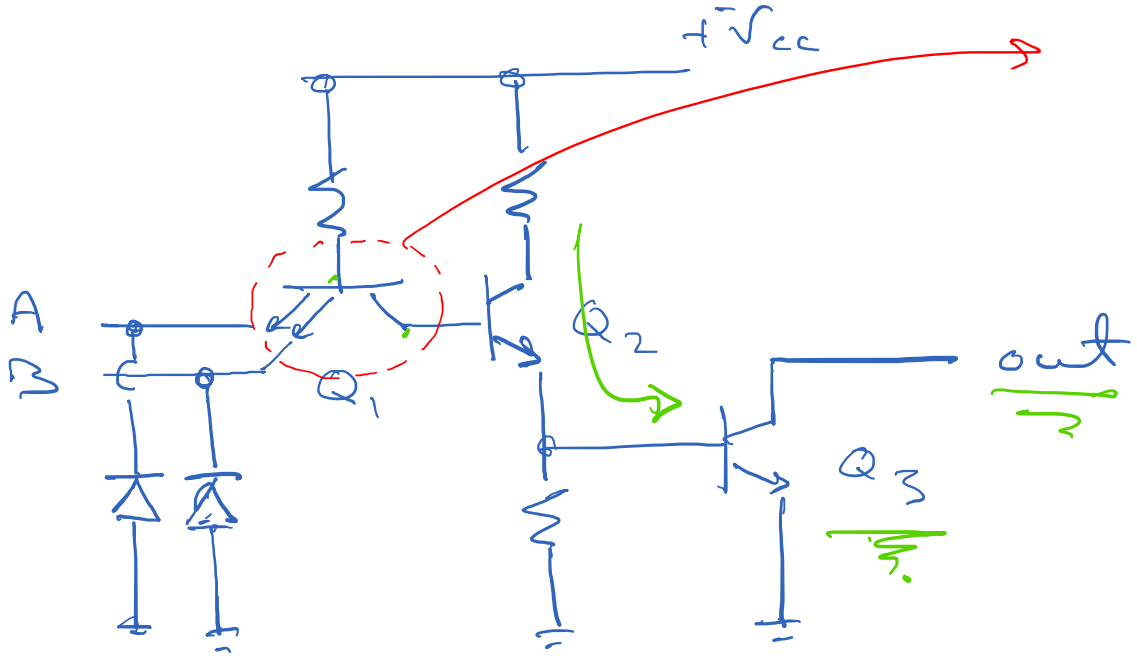
```
      1 0 1
    -------
1 1 | 1 1 1 1
      1 1
    -------
        0 1
          0
        -----
          1 1
```

DIGITAL HARDWARE TTL

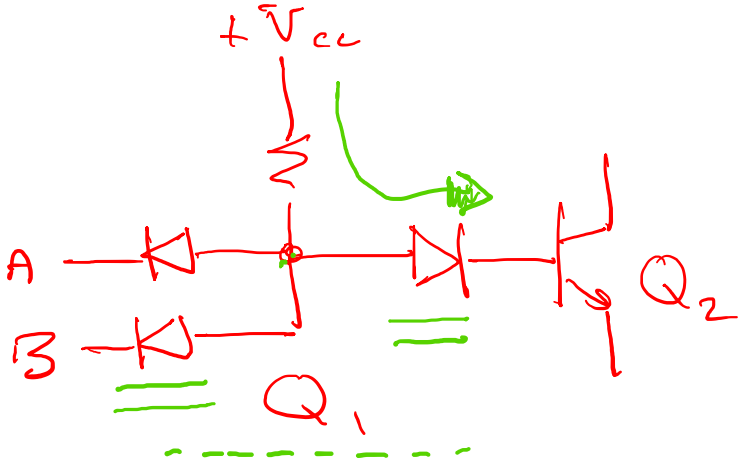
LOGIC LOW → 0 - 0.4 V [NOMINAL 0 V]
LOGIC HIGH → 3 - 5 V [NOM. 4.75 V]
PROPAGATION DELAY ~ 10 nS
FANOUT ~ 10



DIGITAL HARDWARE TTL



A	B	out = $\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0



A OR B IS LOGIC LOW

Q_2 BASE IS PULLED TO GROUND

Q_3 OFF

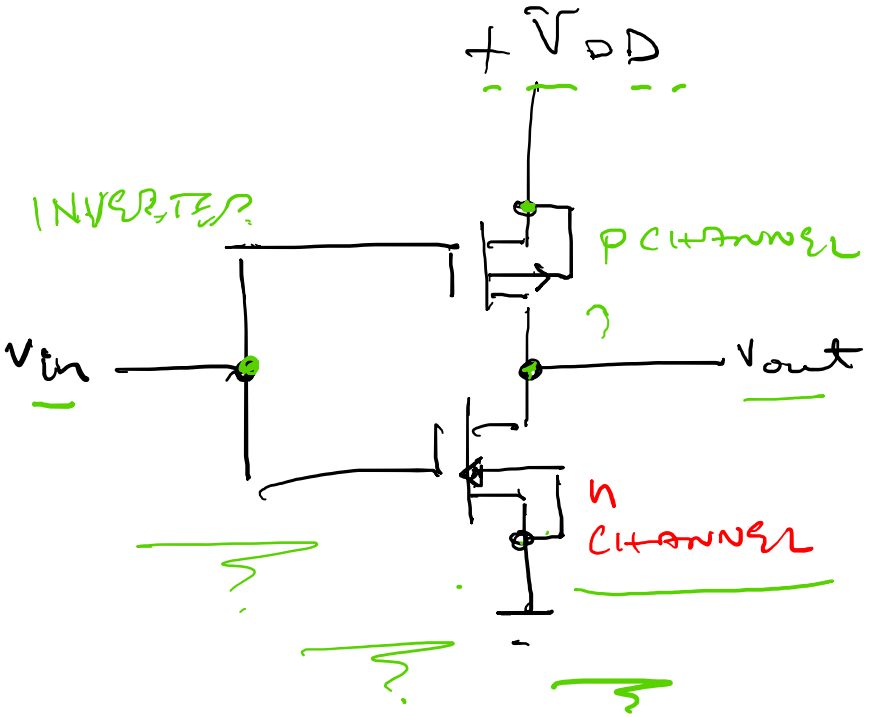
OUTPUT → HIGH

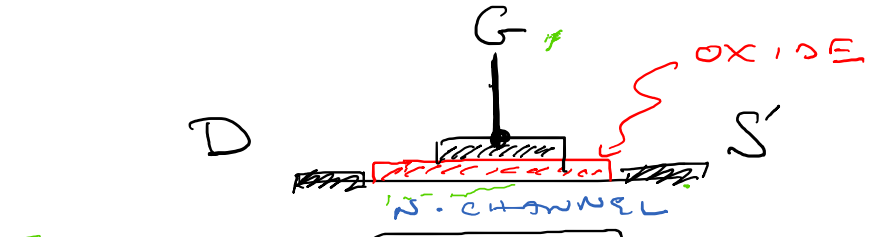
A AND B ARE HIGH → OUTPUT PULLED LOW

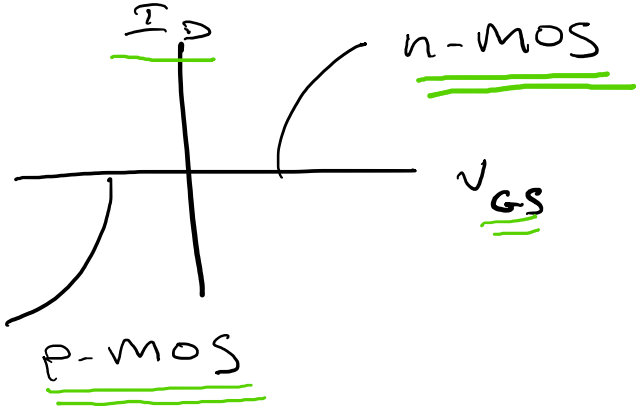
DIGITAL HARDWARE

CMOS

COMPLEMENTARY



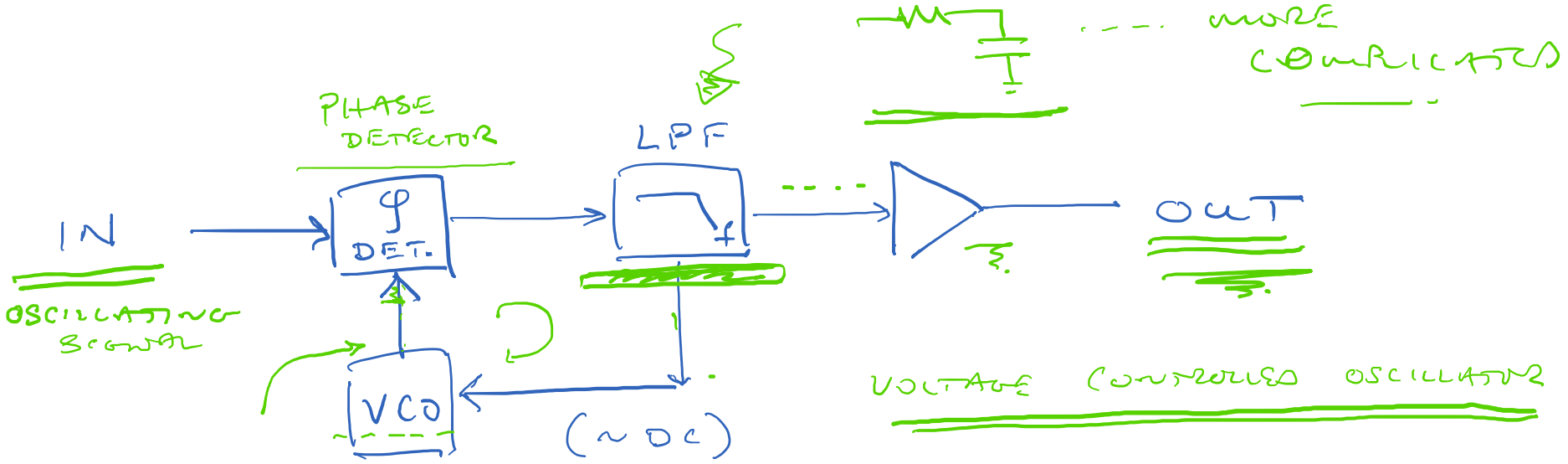




$V_{in} = +1 \rightarrow V_{out} \rightarrow 0$ [n conducts]

$V_{in} = 0 \rightarrow V_{out} \rightarrow 1$

PHASE-LOCKED LOOP



→ NULL DETECTION: NEGATIVE F.B., SO OUTPUT TENDS TO ZERO [APT. FROM SMALL ERROR SIGNAL]

→ DC/LF SIGNAL SENT INTO VCO ENCODES PHASE OF V_{in}

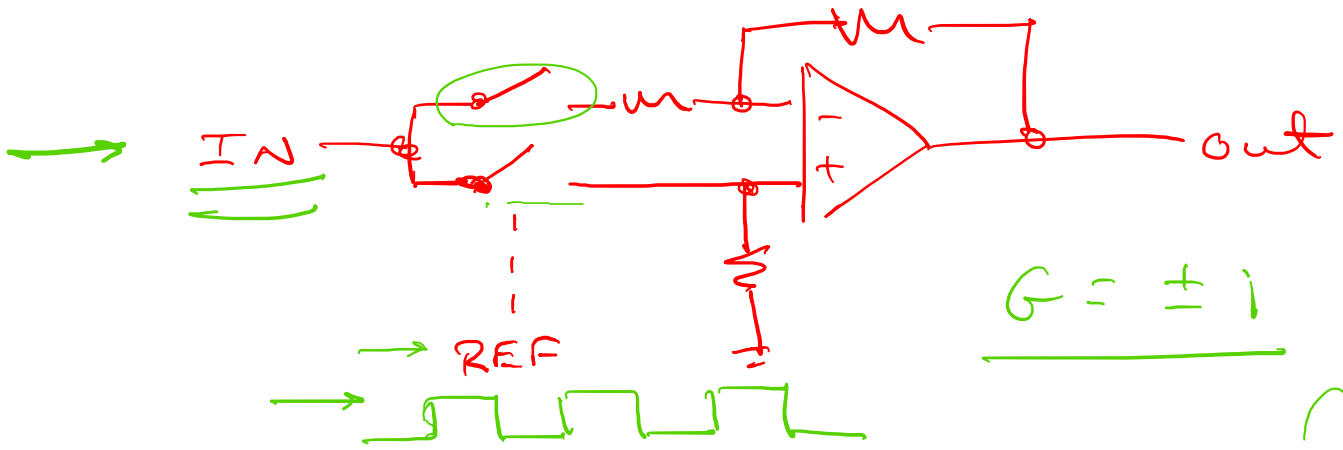
VCO OUTPUT IS "COPY" OF INPUT SIGNAL: CLOCK DISTRIBUTION

PHASE DETECTOR

TYPE I : LEVEL-SENSITIVE

TYPE II : EDGE-SENSITIVE

TYPE I : e.g. SWITCHED FETs w/ OP AMP



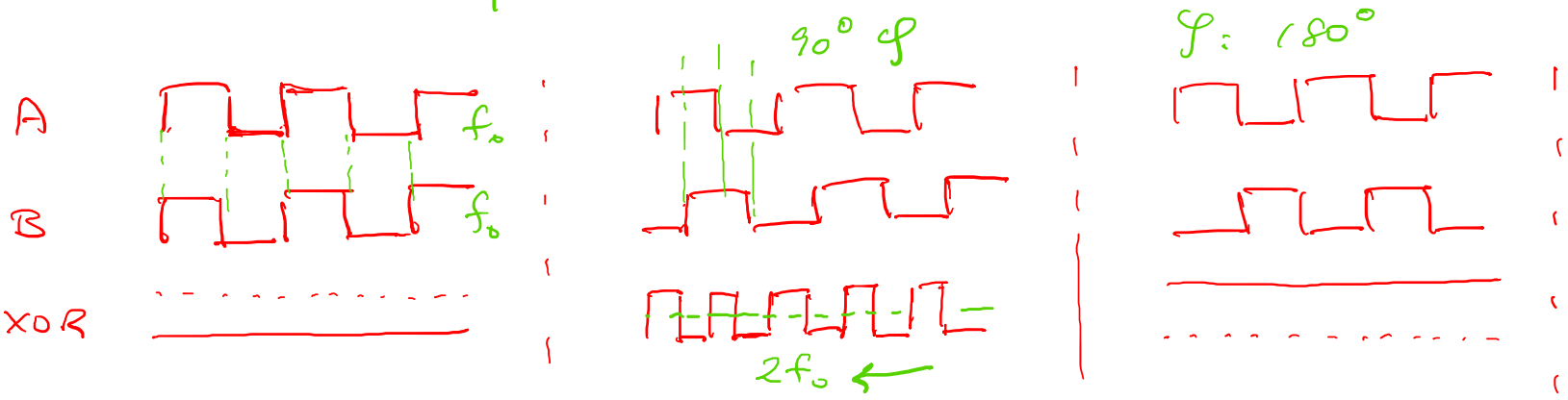
$G = \pm 1$

$\langle out \rangle \neq 0$

ANOTHER POSSIBILITY: DIGITAL COMPARATOR

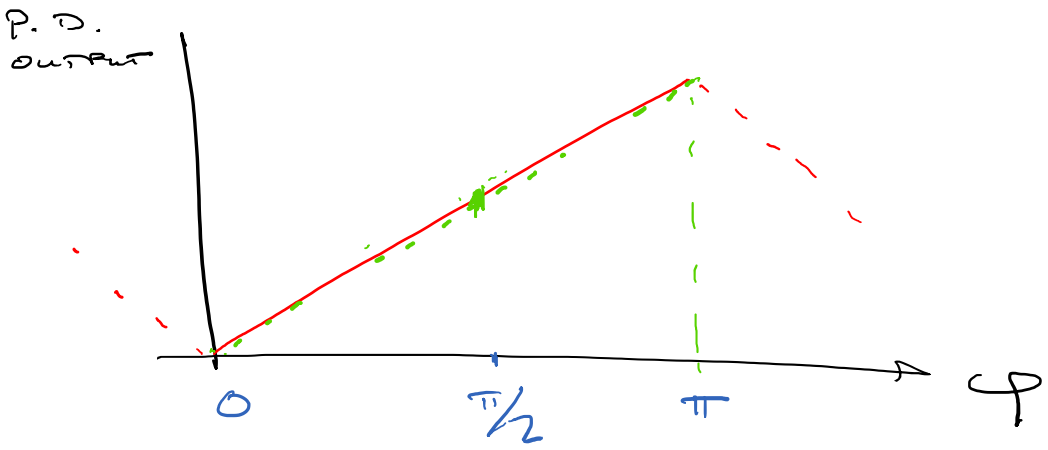
A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

XOR



$$\rightarrow \langle XOR \rangle = \frac{1}{\pi} |\pi - \varphi|$$

DIGITAL PHASE DETECTOR



LOCK RANGE: RANGE OF FREQUENCY OVER WHICH PLL REMAINS LOCKED, PROVIDED IT WAS INITIALLY LOCKED

CAPTURE RANGE: RANGE OF FREQ. OVER WHICH PLL WILL FIND A LOCK.