

SIGNED BINARY MULTIPLICATION

$$\begin{array}{r}
 \\
 b_0 \\
 b_1 \\
 b_2 \\
 \times \\
 \hline
 b_0 a_0 \\
 b_1 a_0 \\
 b_2 a_0 \\
 b_0 a_1 \\
 b_1 a_1 \\
 b_2 a_1 \\
 b_0 a_2 \\
 b_1 a_2 \\
 b_2 a_2 \\
 \hline
 b_0 a_0 \\
 b_0 a_1 \\
 b_0 a_2 \\
 b_1 a_0 \\
 b_1 a_1 \\
 b_1 a_2 \\
 b_2 a_0 \\
 b_2 a_1 \\
 b_2 a_2 \\
 \hline
 \text{etc.}
 \end{array}$$

The diagram illustrates the bit-by-bit multiplication process. Red arrows and squiggly lines indicate the flow of partial products from the multiplicand (a₂a₁a₀) and multiplier (b₂b₁b₀) to the resulting partial products. A red arrow points to the first partial product row (b₀a₀), and another points to the second row (b₁a₀ b₀a₁). A red squiggly line on the left indicates the continuation of the process.

e.g. $\underline{\underline{3 \times (-3)}}$

$$\begin{array}{r} 0 \quad 1 \quad 1 \\ \hline \times \quad 1 \quad 0 \quad 1 \\ \hline \rightarrow 0 \quad 1 \quad 1 \end{array}$$

$$0 \quad 0 \quad 0$$

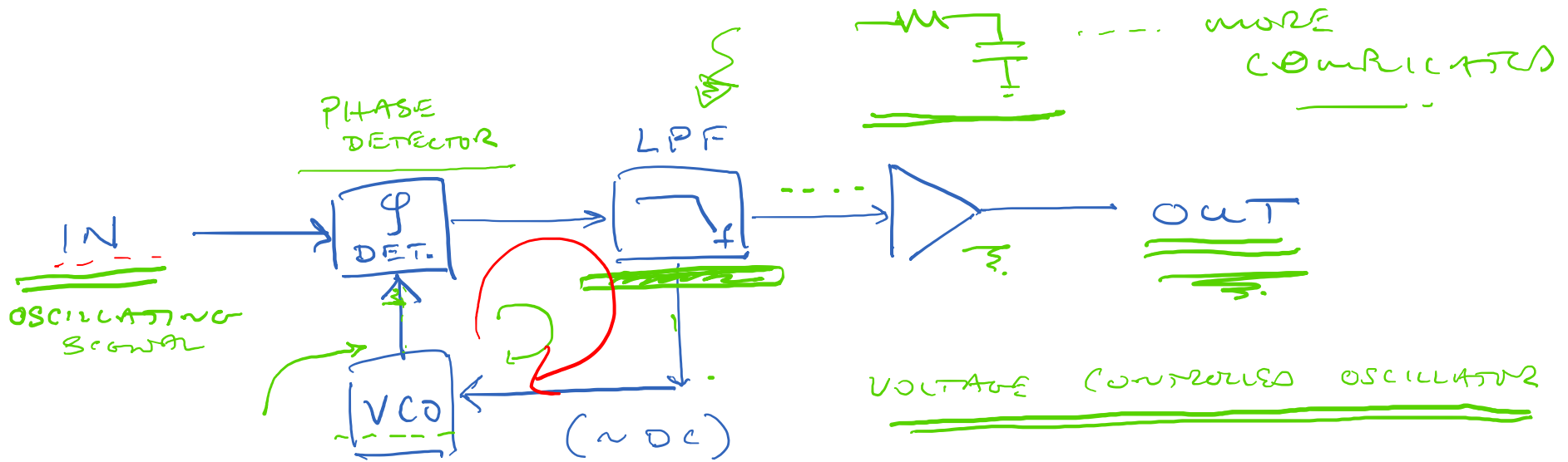
$$\underline{0 \quad 1 \quad 1}$$

$$\begin{array}{r} + \quad 1 \quad 0 \quad 1 \\ \hline 1 \quad 1 \quad 0 \quad 1 \quad 1 \end{array}$$

11

0.11

PHASE-LOCKED LOOP



→ NULL DETECTION: NEGATIVE F.B., SO OUTPUT TENDS TO ZERO [APT. FROM SMALL ERROR SIGNAL]

→ DC/LF SIGNAL SENT INTO VCO ENCODES PHASE OF VIN

VCO OUTPUT IS "COPY" OF INPUT SIGNAL: CLOCK DISTRIBUTION

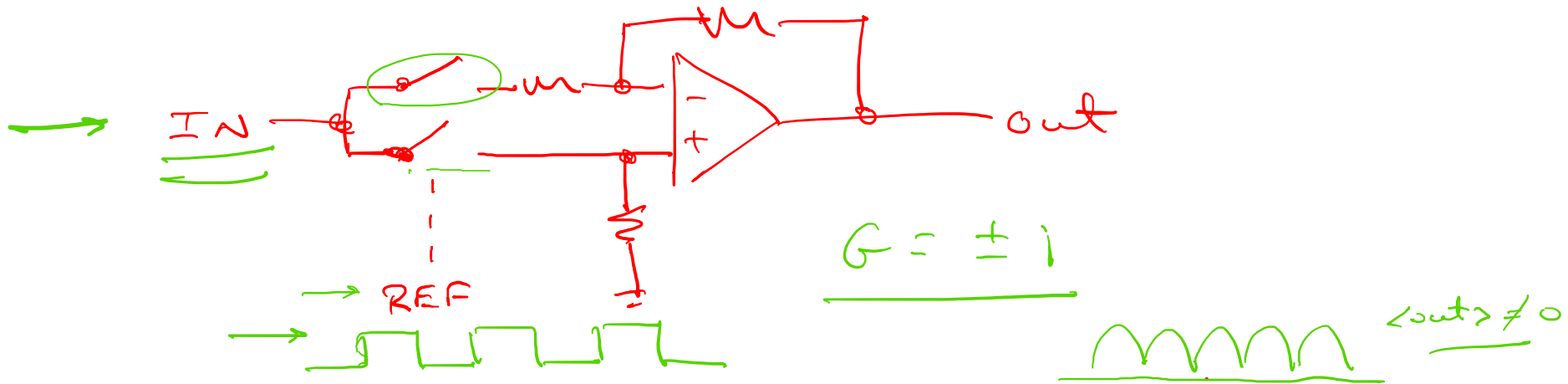
PHASE DETECTOR

TYPE I : LEVEL-SENSITIVE ←

TYPE II : EDGE-SENSITIVE

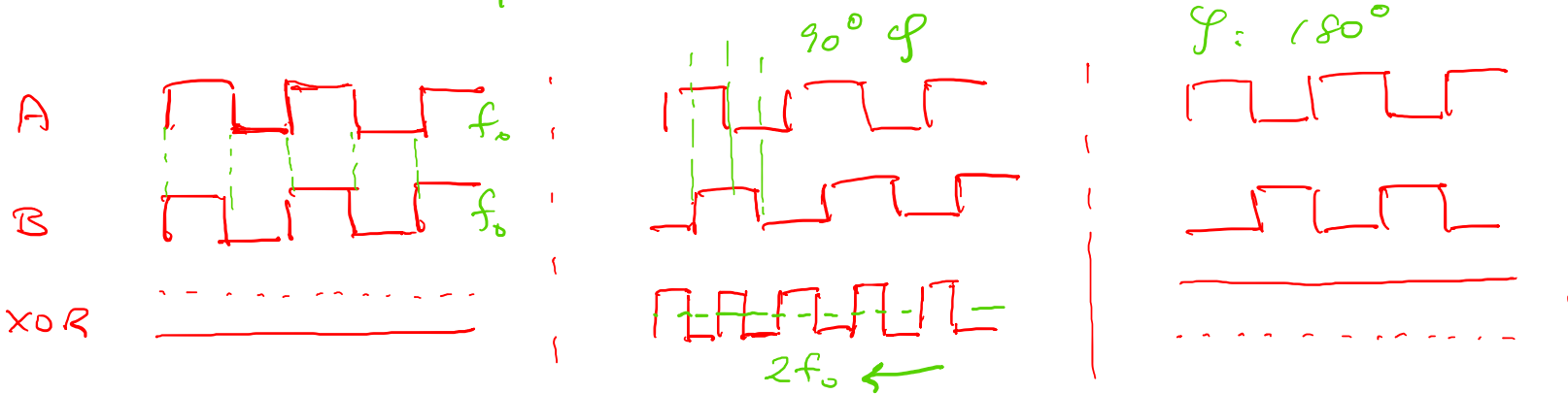
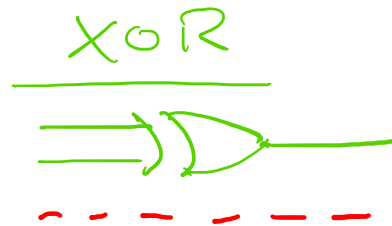
SWAMP

TYPE I : e.g. SWITCHED FETs w/ OP AMP



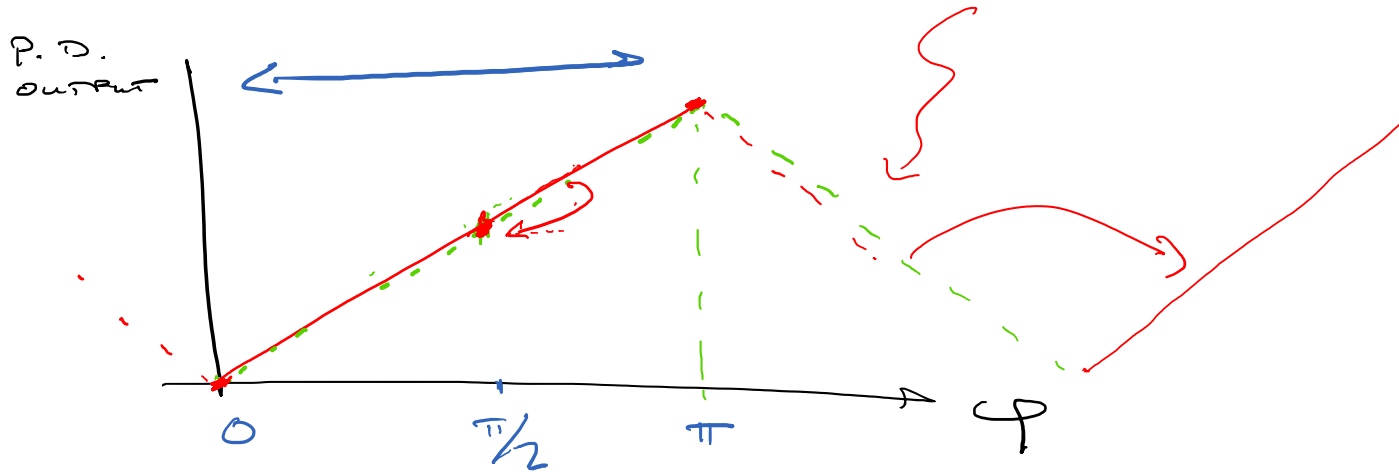
ANOTHER POSSIBILITY: DIGITAL COMPARATOR

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0



$\rightarrow \langle \text{XOR} \rangle = \frac{1}{\pi} |\pi - \varphi|$

DIGITAL PHASE DETECTOR



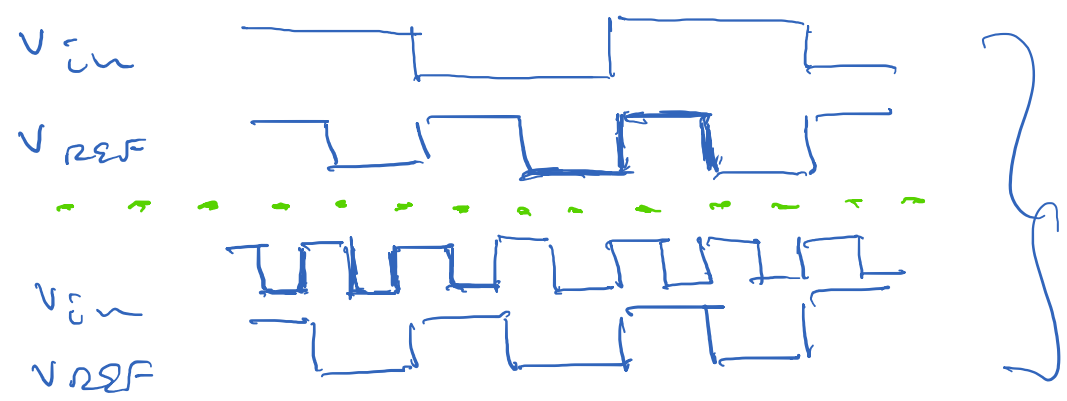
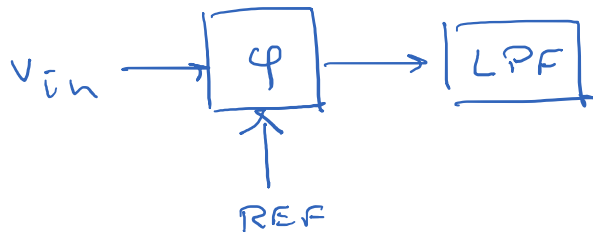
LOCK RANGE:

RANGE OF FREQUENCY OVER WHICH PLL REMAINS LOCKED,
PROVIDED IT WAS INITIALLY LOCKED.

CAPTURE RANGE:

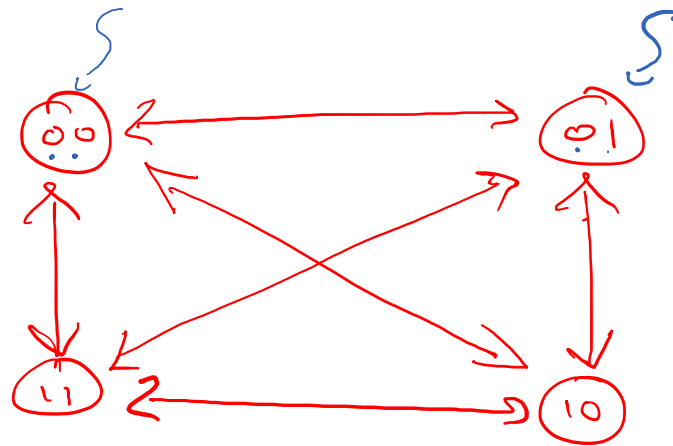
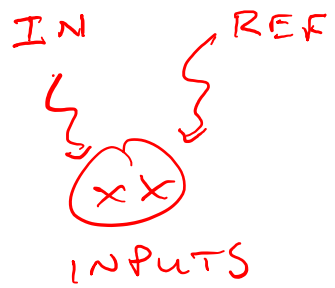
RANGE OF FREQ. OVER WHICH PLL WILL FIND
A LOCK.

TYPE I P.D. LOCK @ (SUB) HARMONICS



In BOTH CASES,
 $\langle XOR \rangle = \frac{1}{2}$

TYPE I P.D. : STATE DIAGRAM



OUTPUTS

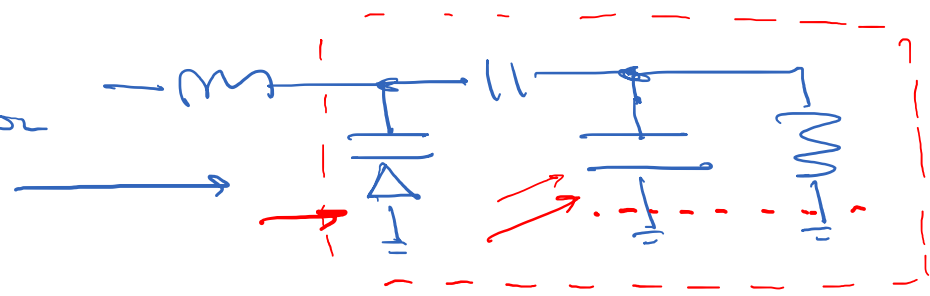


VOLTAGE CONTROLLED OSCILLATOR

SEE H+H
13.94 + DISCUSSION

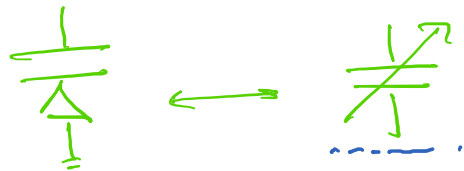
e.g.

VCO CONTROL

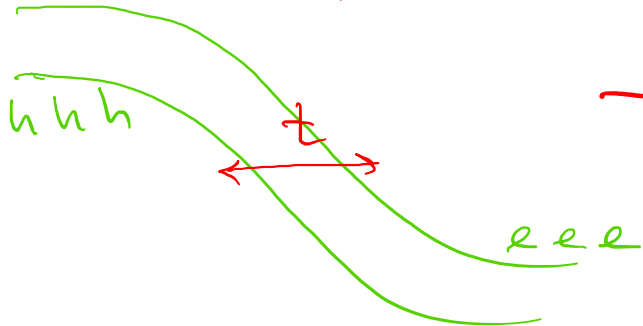


OSCILLATOR
TANK CIRCUIT
SETS FREQUENCY
OF CAPACITORS/INDUCTOR
OSCILLATOR

VARACTOR DIODE



REVERSE-BIASED PN JUNCTION
WIDTH OF DEPLETION REGION CONTROLLED
BY EXTERNAL VOLTAGE.



DEPLETION WIDTH $t \propto V^{1/2}$

$C \propto V^{-1/2}$

PF $\rightarrow \sim 1000$ pF

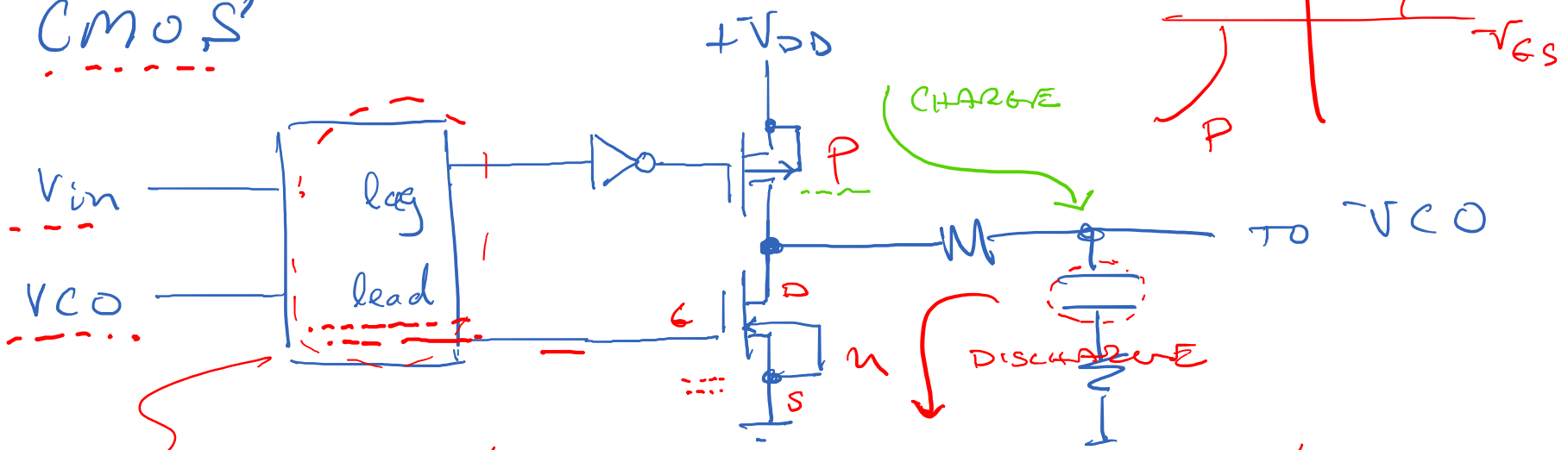
TUNING RANGE
 $\sim 3:1$

\downarrow
 $\sim 15:1$

TYPE II P.D.

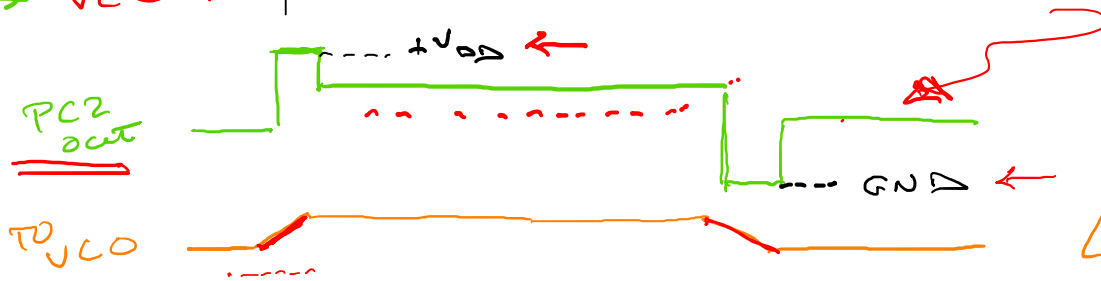
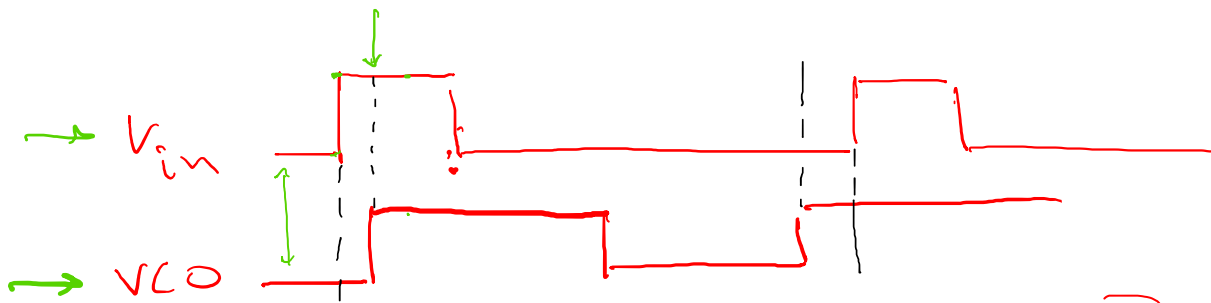
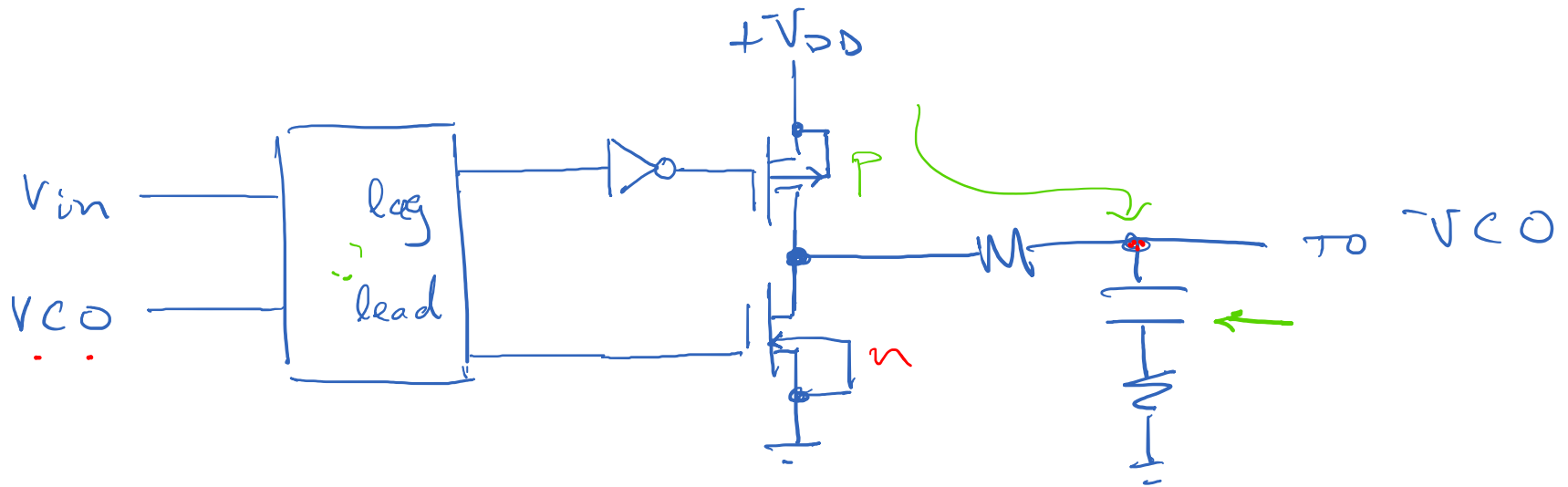
[EDGE-SENSITIVE]

CMOS

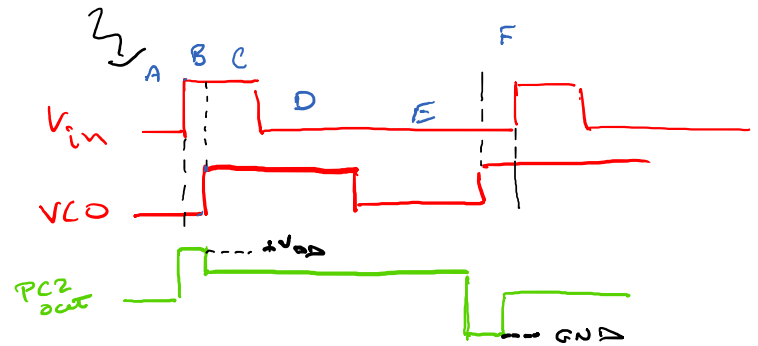
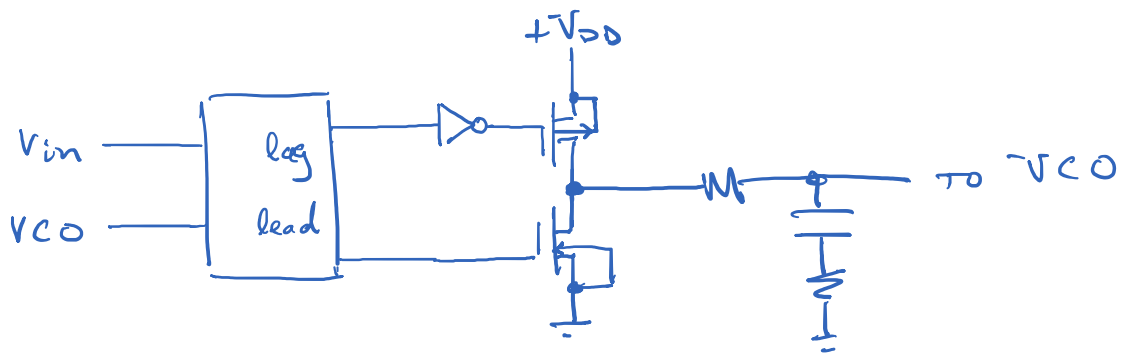


→ CHARGE/DISCHARGE CAP
DEPENDING ON WHETHER INPUT LEADS/LAGS VCO

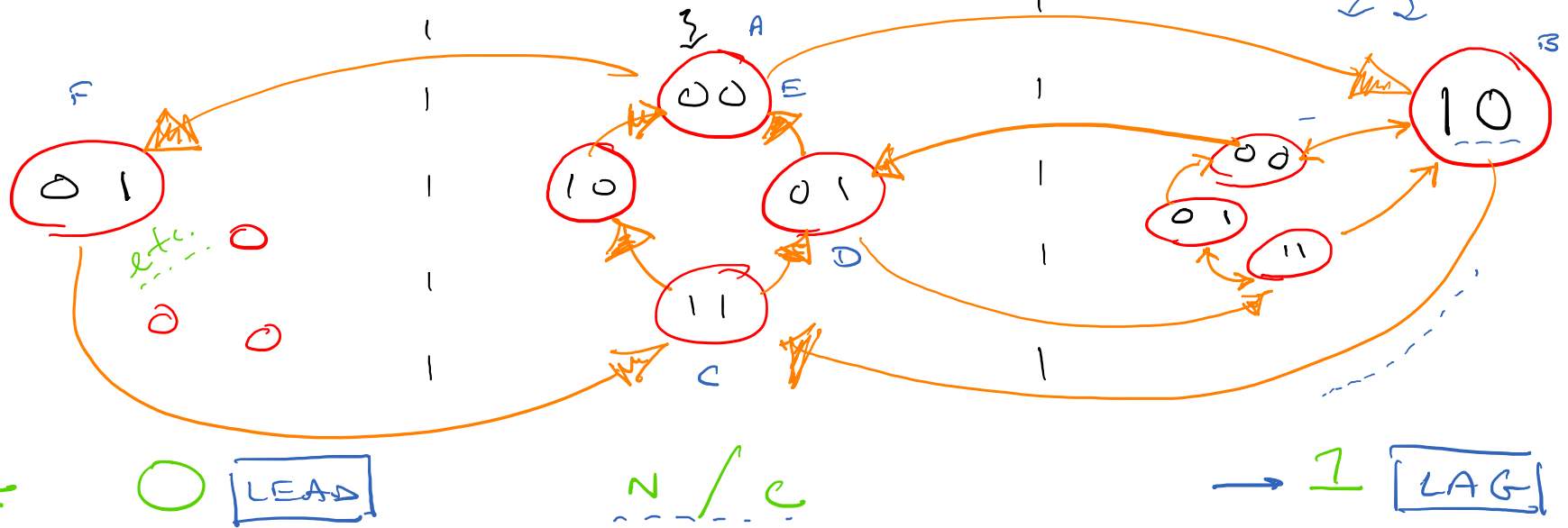
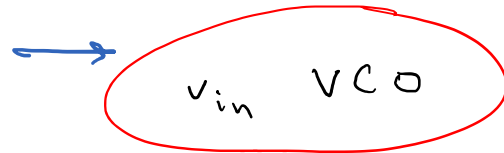
→ INTERNAL DIGITAL LOGIC ("STATE MACHINES")



$[CONST. \frac{dV}{dt} FROM CURRENT SOURCE]$



INTERNAL LOGIC



$PC2_{out}$

PHASE DETECTOR COMPARISON

TYPE I

TYPE II

INPUT DUTY CYCLE

50%

IRRELEVANT

LOCK ON HARMONIC?

YES

NO

NOISE REJECTION

GOOD

POOR

RIPPLE @ $2f_{in}$

HIGH

LOW

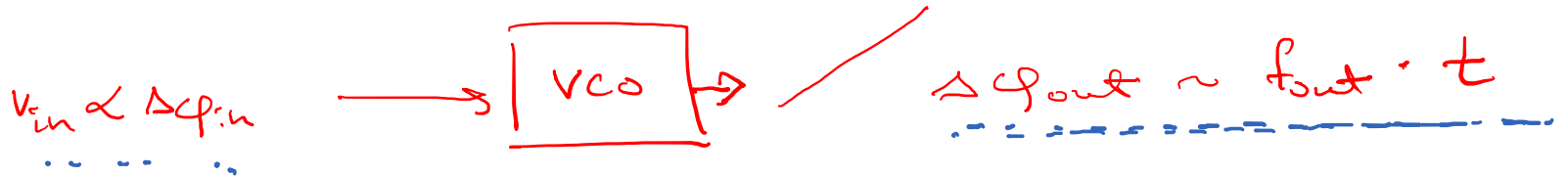
CAPTURE RANGE

$f_c \leq f_{lock}$

$f_c = f_{lock}$

LOOP STABILITY

KEY POINT: VCO INTEGRATES PHASE ERROR



→ LIKE A SINGLE-POLE RC LOW-PASS / INTEGRATOR
 → INTEGRATOR 90° DEG. PHASE SHIFT [FACTOR $\frac{1}{j\omega}$]

LOOP GAIN: ~~XXXXXXXXXX~~

$$K_P \cdot K_F \cdot \frac{K_{VCO}}{j\omega}$$

VOLTS/RAD (above K_P) DIM. LESS (above K_F) RAD/S/VOLT (above K_{VCO})

