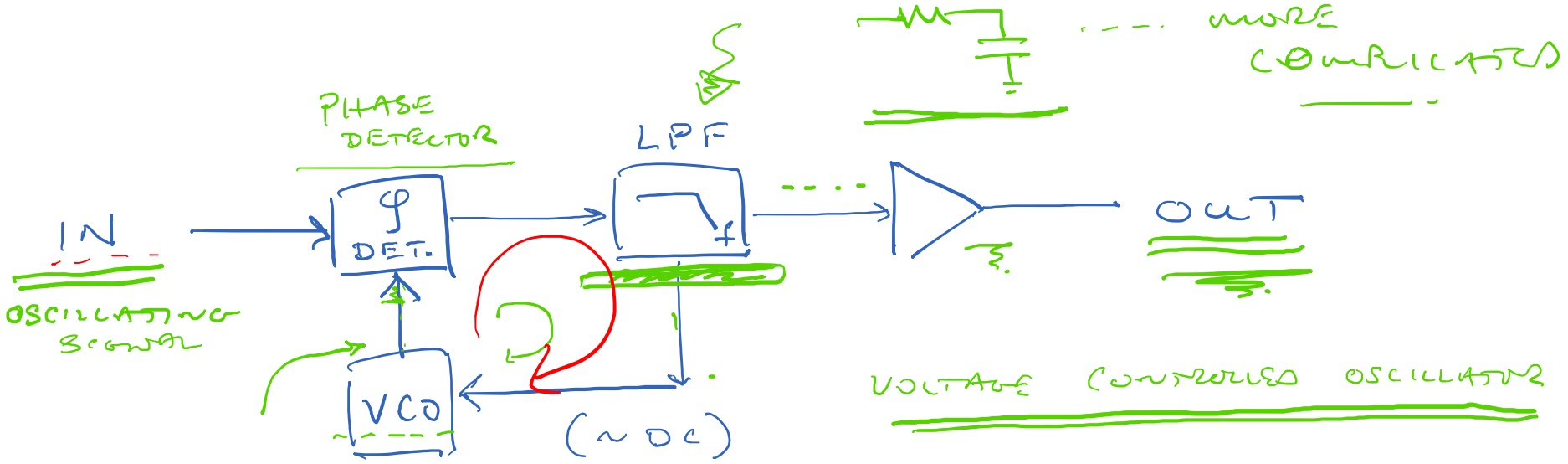
SIGNED BINARY MULTIPLICATION

$$
\begin{array}{rccc}
 & b_2 & b_1 & b_0 \\
\times & a_2 & a_1 & a_0 \\
\hline
\rightarrow & b_2 a_0 & b_1 a_0 & b_0 a_0 \\
 & b_2 a_1 & b_1 a_1 & b_0 a_1 \\
\rightarrow & b_2 a_2 & b_1 a_2 & b_0 a_2 \\
- & (b_2 a_2 & b_1 a_2 & b_0 a_2) \\
\hline
 & \multicolumn{3}{c}{\text{etc.}}
\end{array}
$$

e.g. $-3 \times (-3)$

$$
\begin{array}{r}
0.1.1. \\
\times\ 1\ 0\ 1 \\
\hline
0\ 1\ 1 \\
0\ 0\ 0\ . \\
0\ 1\ 1\ . \\
+\ 1\ 0\ 1 \\
\hline
1\ 1\ 0\ 1\ 1\ 1
\end{array}
= -9
$$

PHASE-LOCKED LOOP



→ NULL DETECTION: NEGATIVE F.B., SO OUTPUT TENDS TO ZERO [APT. FROM SMALL ERROR SIGNAL]

→ DC/LF SIGNAL SENT INTO VCO ENCODES PHASE OF V_{in}

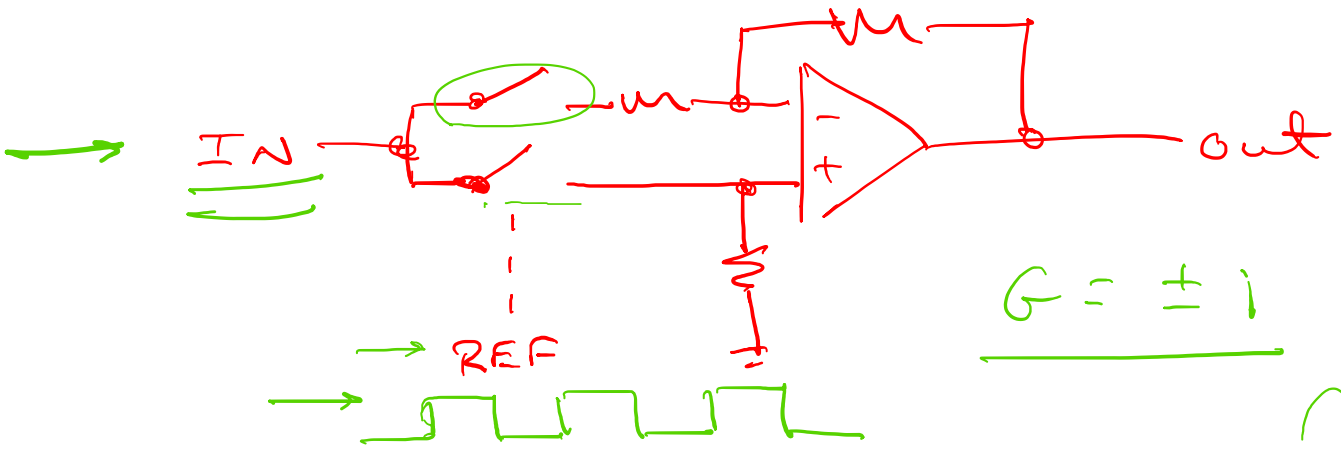
VCO OUTPUT IS "COPY" OF INPUT SIGNAL: CLOCK DISTRIBUTION

PHASE DETECTOR

TYPE I : LEVEL-SENSITIVE ←

TYPE II : EDGE-SENSITIVE

TYPE I : e.g. SWITCHED FETs w/ OP AMP



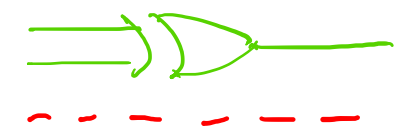
G = ± 1

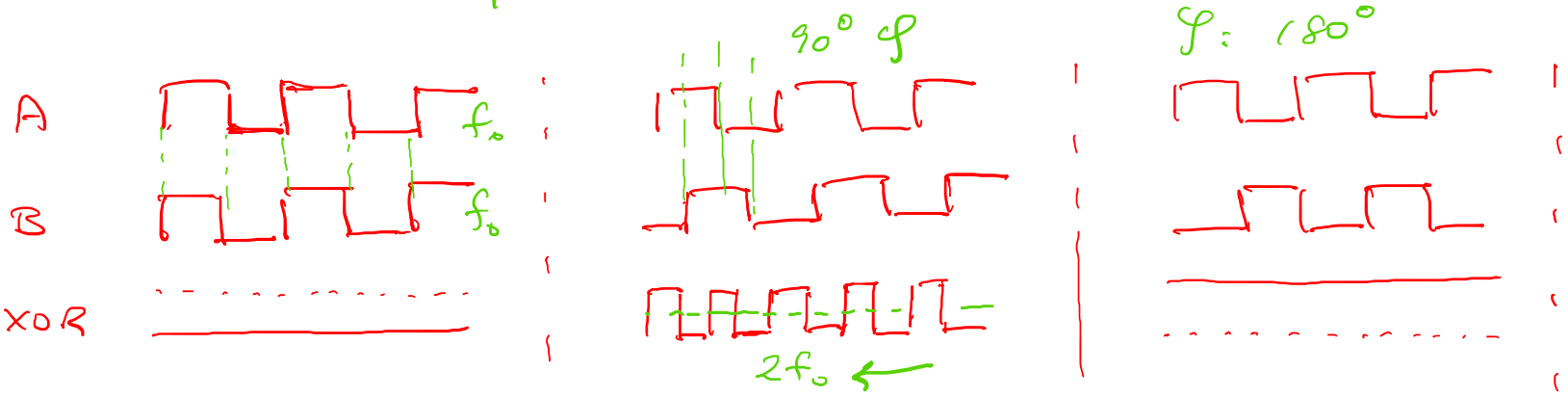
<out> ≠ 0

ANOTHER POSSIBILITY: DIGITAL COMPARATOR

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

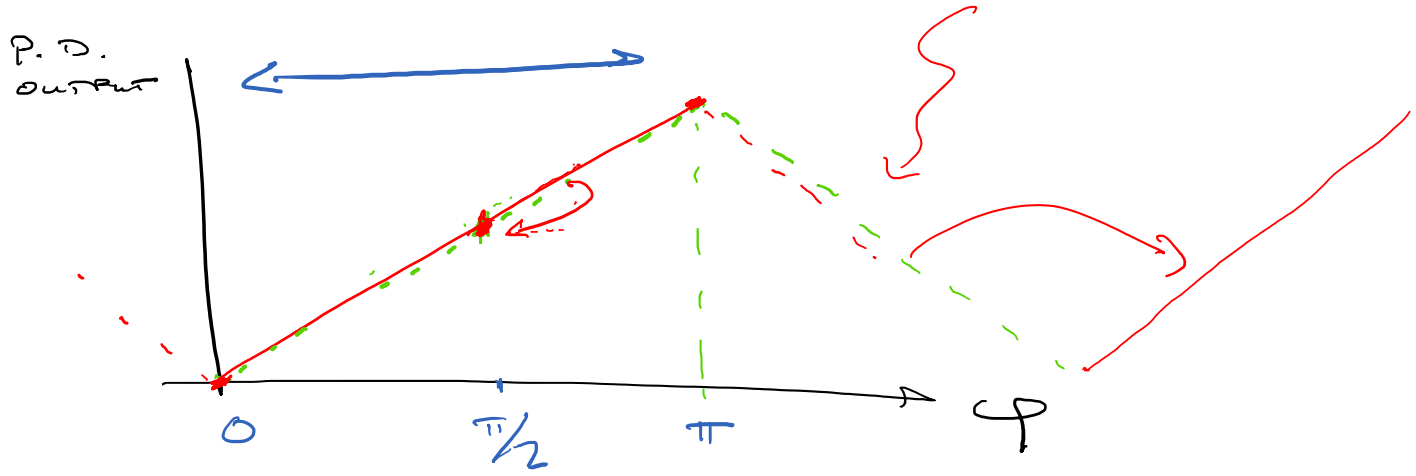
XOR





$$\longrightarrow \langle XOR \rangle = \frac{1}{\pi} |\pi - \varphi|$$

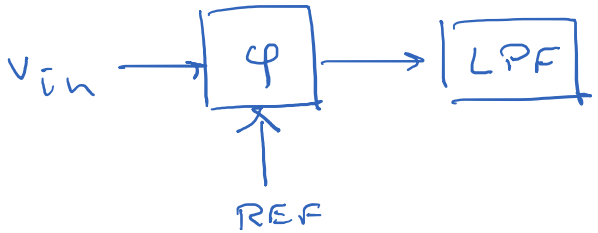
DIGITAL PHASE DETECTOR

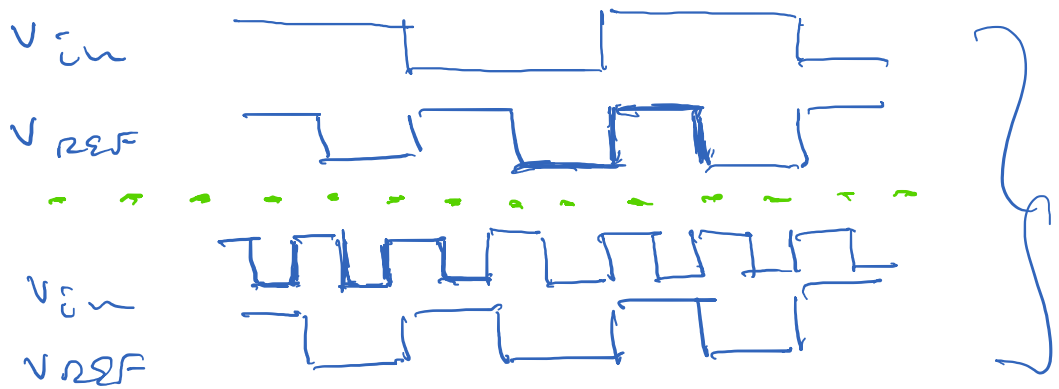


LOCK RANGE: RANGE OF FREQUENCY OVER WHICH PLL REMAINS LOCKED, PROVIDED IT WAS INITIALLY LOCKED

CAPTURE RANGE: RANGE OF FREQ. OVER WHICH PLL WILL FIND A LOCK.

TYPE I P.D. : LOCK @ (SUB) HARMONICS

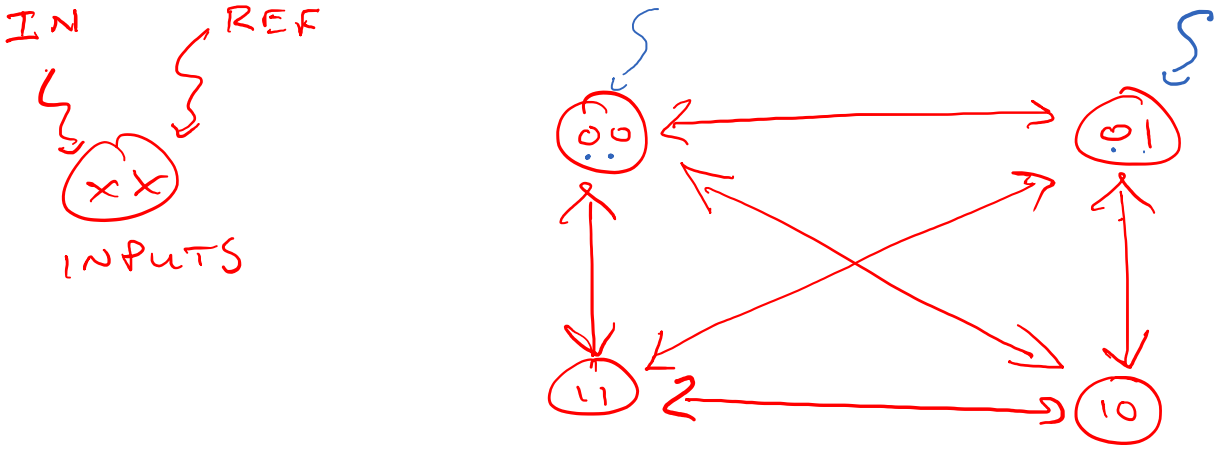




In Both CASES,

$\langle XOR \rangle = \frac{1}{2}$

TYPE I P.D. : STATE DIAGRAM

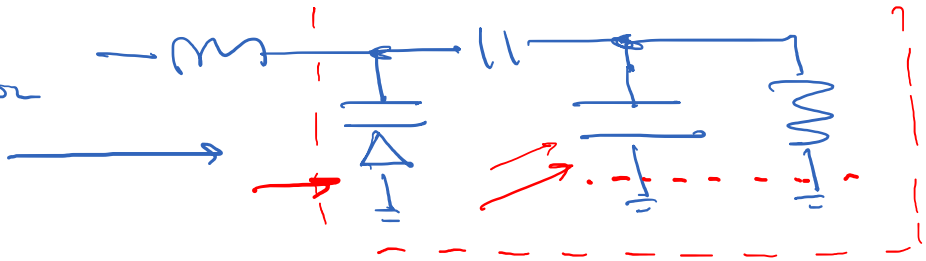


OUTPUTS 0 1

⇒ VOLTAGE CONTROLLED OSCILLATOR

⇒ [SEE H+H 13.94 + DISCUSSION]

e.g. VCO CONTROL →

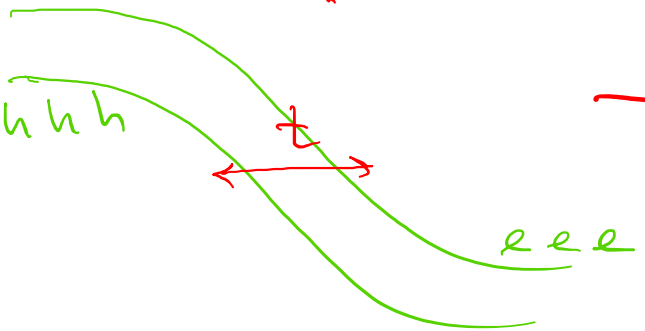


OSCILLATOR TANK CIRCUIT [SETS FREQUENCY OF COLPITTS/HARTLEY OSCILLATOR]

VARACTOR DIODE

REVERSE-BIASED pn JUNCTION
WIDTH OF DEPLETION REGION CONTROLLED BY EXTERNAL VOLTAGE.

P ANODE → |‖ — n CATHODE



→ DEPLETION WIDTH $t \propto V^{1/2}$

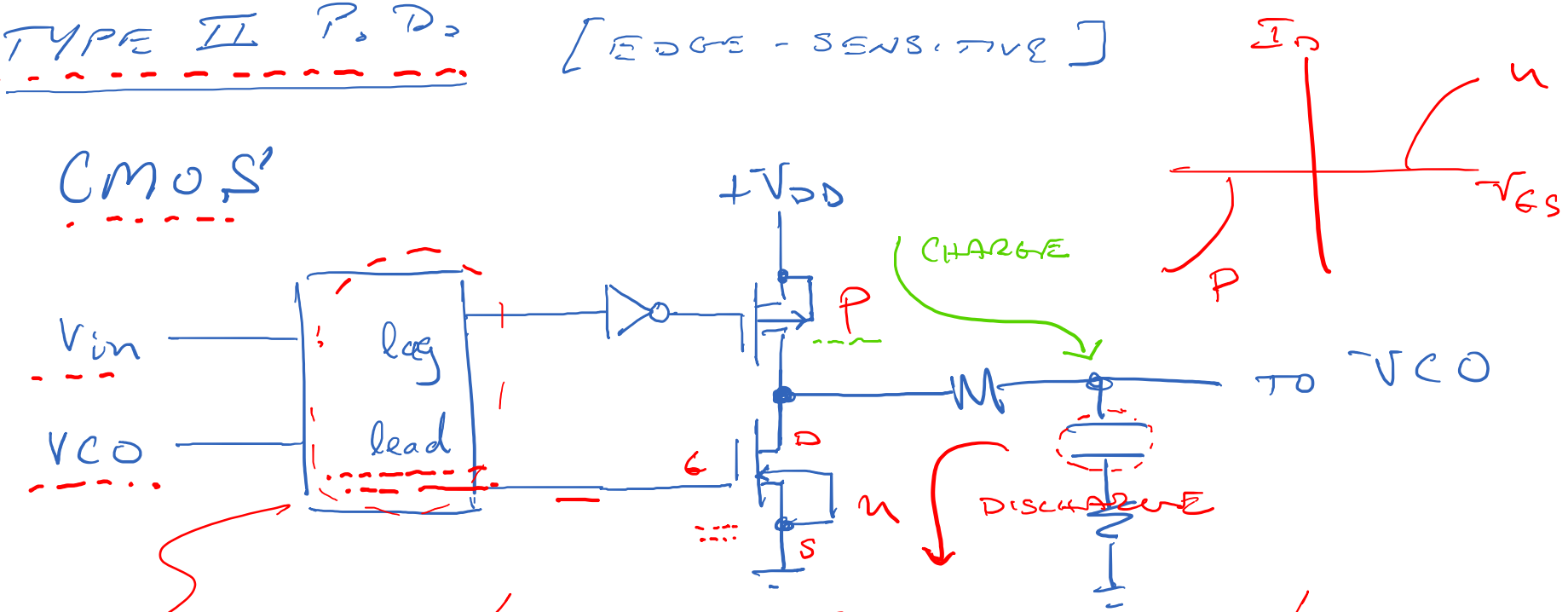
$C \propto V^{-1/2}$

→ pF → ~100s pF

TUNING RANGE
~3:1
⋮
~15:1

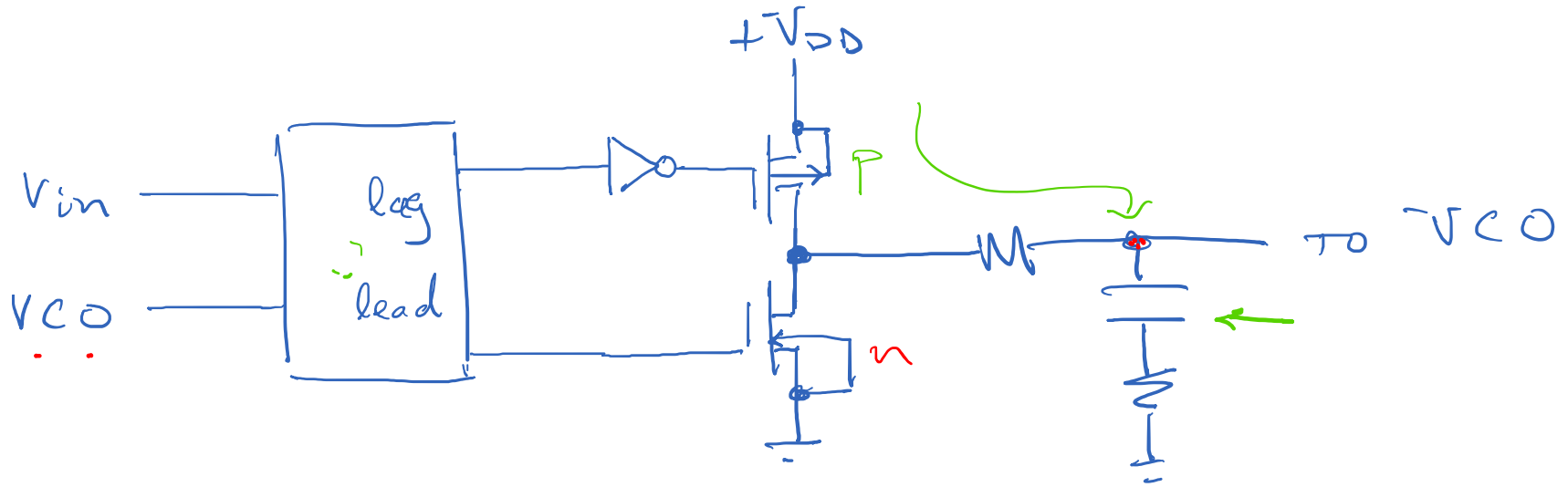
TYPE II P.D. [EDGE-SENSITIVE]

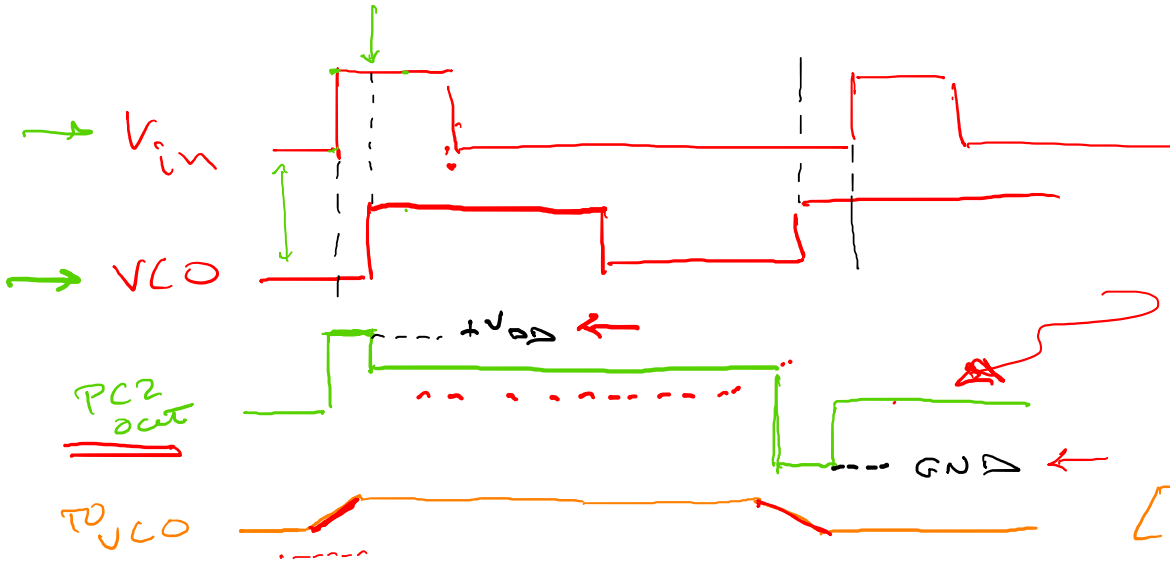
CMOS



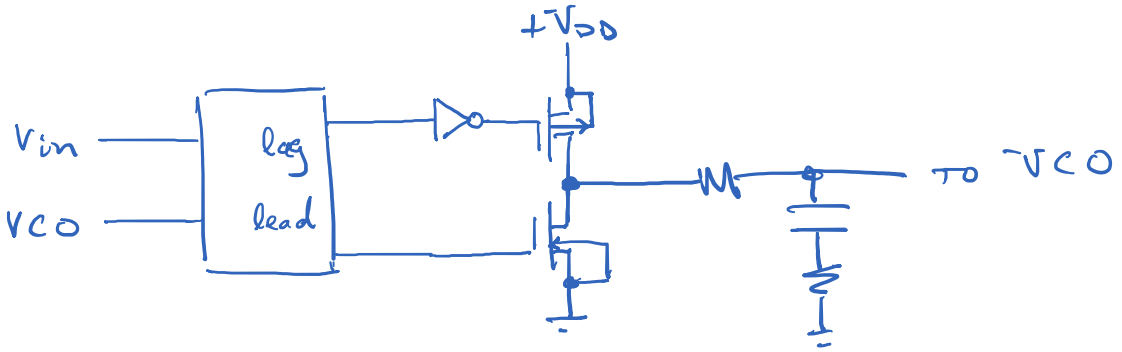
→ CHARGE/DISCHARGE CAP DEPENDING ON WHETHER INPUT LEADS/LAGS VCO

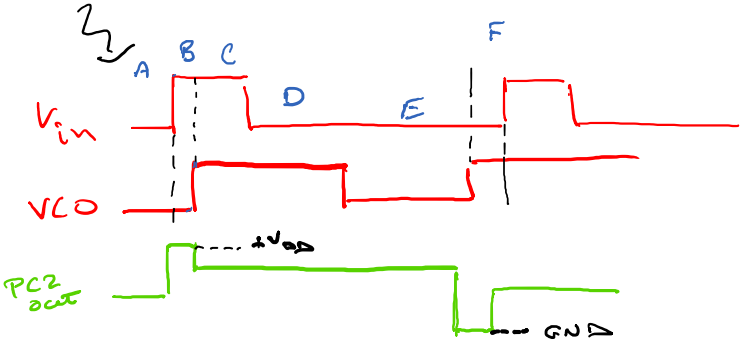
INTERNAL DIGITAL LOGIC ("STATE MACHINE")



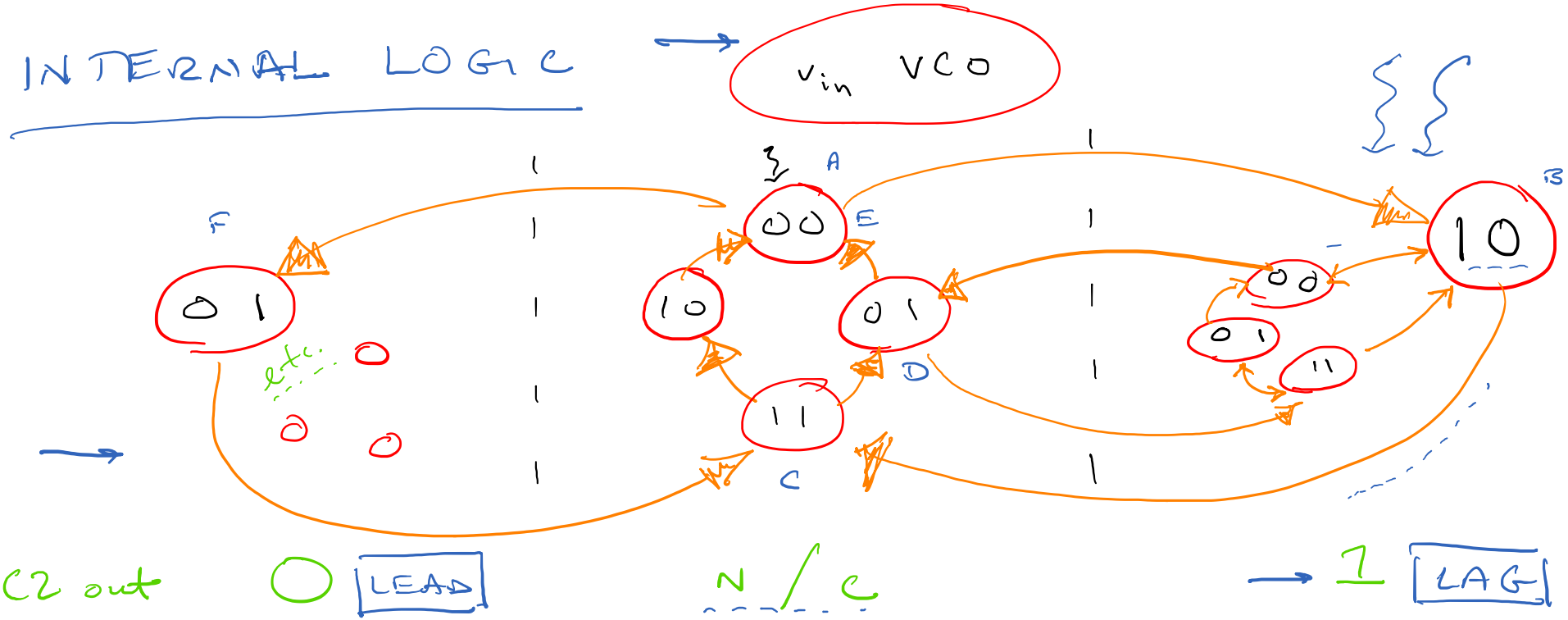


[CONST. $\frac{dV}{dt}$ FROM CURRENT SOURCE]





INTERNAL LOGIC

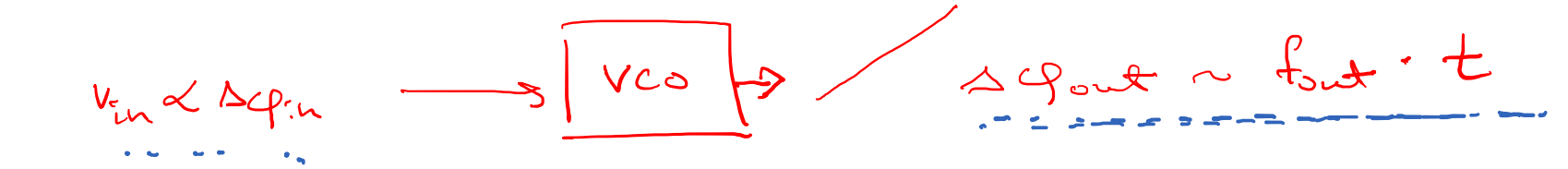


Phase Detector Comparison

	Type I	Type II
Input Duty Cycle	50%	Irrelevant
Lock on Harmonic?	Yes	No
Noise Rejection	Good	Poor
Ripple @ $2f_{in}$	High	Low
Capture Range	$f_c \leq f_{lock}$	$f_c = f_{lock}$

LOOP STABILITY

KEY POINT: VCO INTEGRATES PHASE ERROR



→ LIKE A SINGLE-POLE RC LOW-PASS / INTEGRATOR

→ INHERENT 90° DEG. PHASE SHIFT [FACTOR $\frac{1}{j\omega}$]

LOOP GAIN:

K_P (VOLTS/RAD) · K_F (DIM. LESS) · K_{VCO} (RAD/S / VOLT) · $\frac{1}{j\omega}$ ←