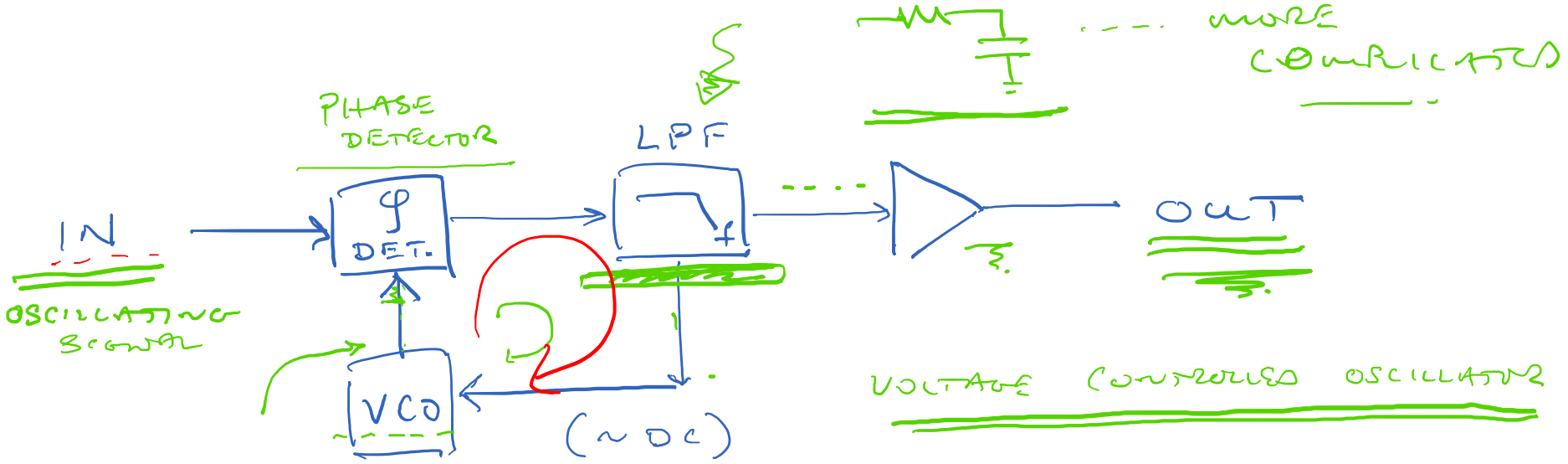
PHASE-LOCKED LOOP



→ NULL DETECTION: NEGATIVE F.B., SO OUTPUT TENDS TO ZERO [APT. FROM SMALL ERROR SIGNAL]

→ DC/LF SIGNAL SENT INTO VCO ENCODES PHASE OF V_{in}

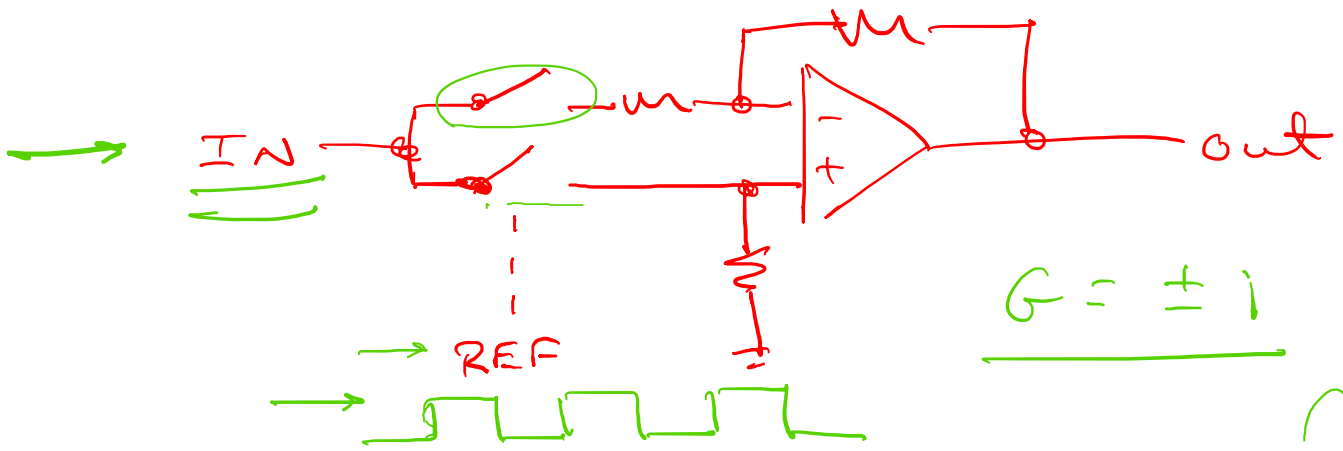
VCO OUTPUT IS "COPY" OF INPUT SIGNAL: CLOCK DISTRIBUTION

PHASE DETECTOR

TYPE I : LEVEL-SENSITIVE ←

TYPE II : EDGE-SENSITIVE

TYPE I : e.g. SWITCHED FETs w/ OP AMP



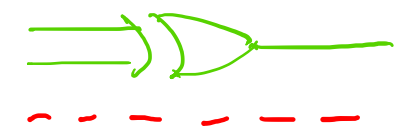
$G = \pm 1$

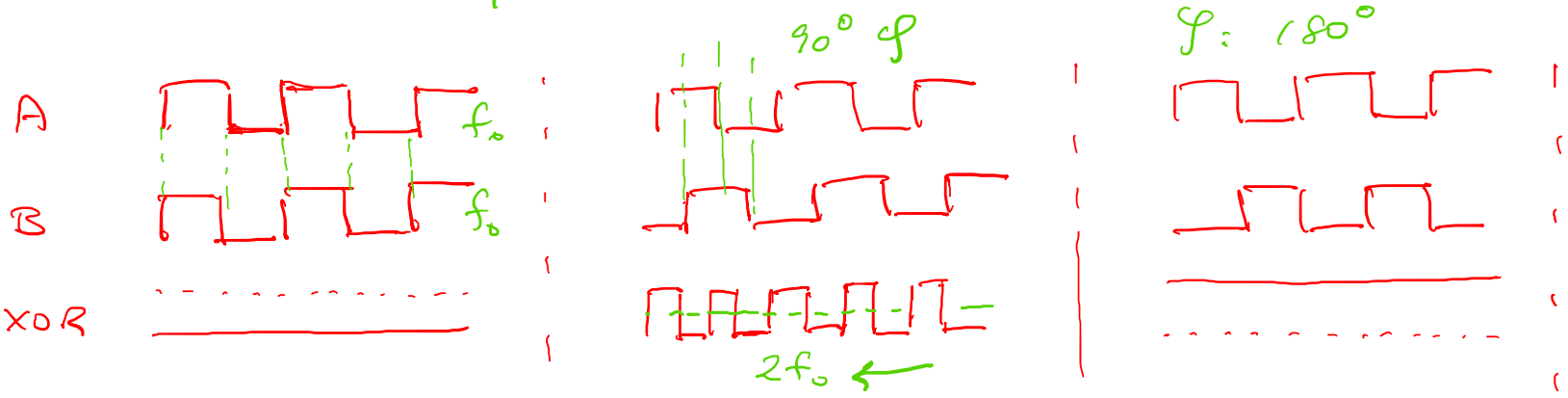
$\langle out \rangle \neq 0$

ANOTHER POSSIBILITY: DIGITAL COMPARATOR

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

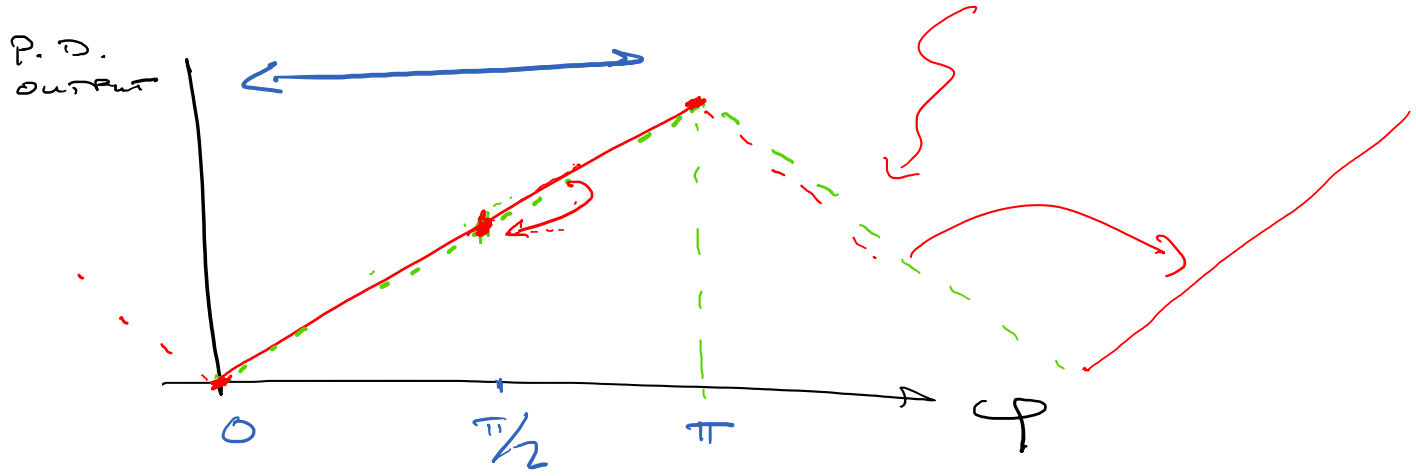
XOR





$$\longrightarrow \langle XOR \rangle = \frac{1}{\pi} |\pi - \varphi|$$

DIGITAL PHASE DETECTOR

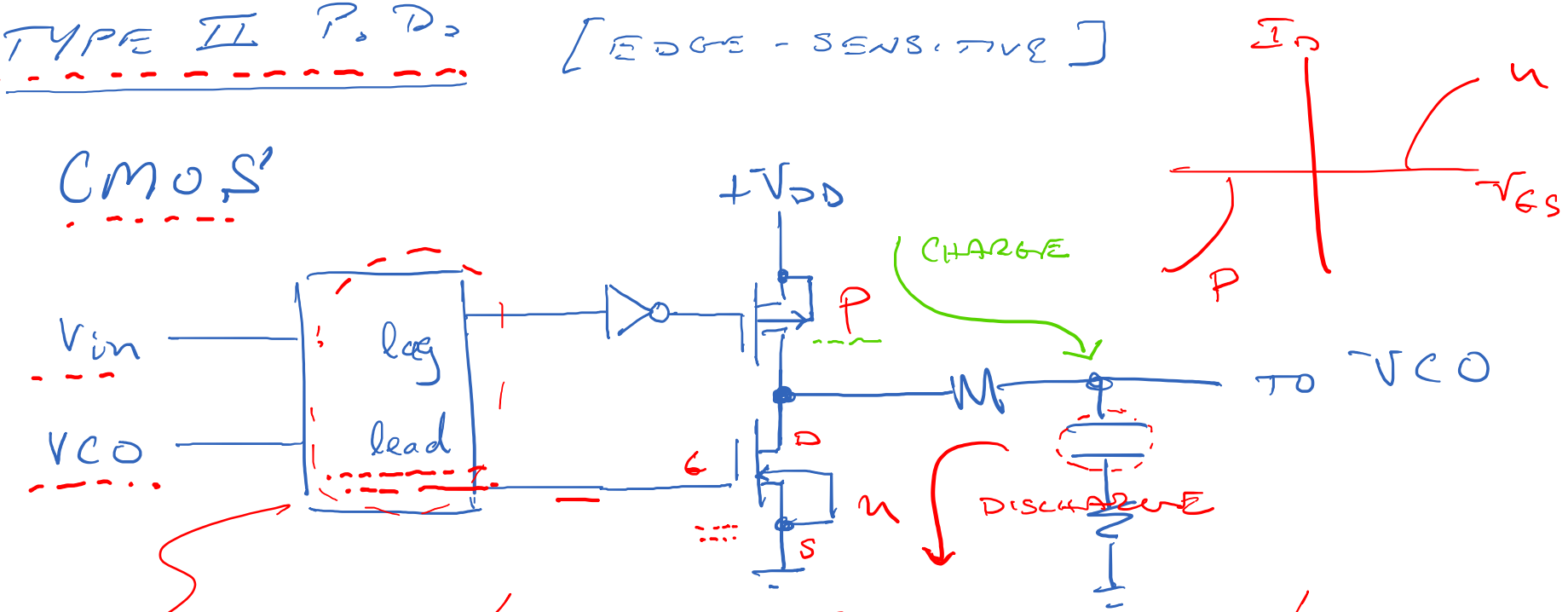


LOCK RANGE: RANGE OF FREQUENCY OVER WHICH PLL REMAINS LOCKED, PROVIDED IT WAS INITIALLY LOCKED

CAPTURE RANGE: RANGE OF FREQ. OVER WHICH PLL WILL FIND A LOCK.

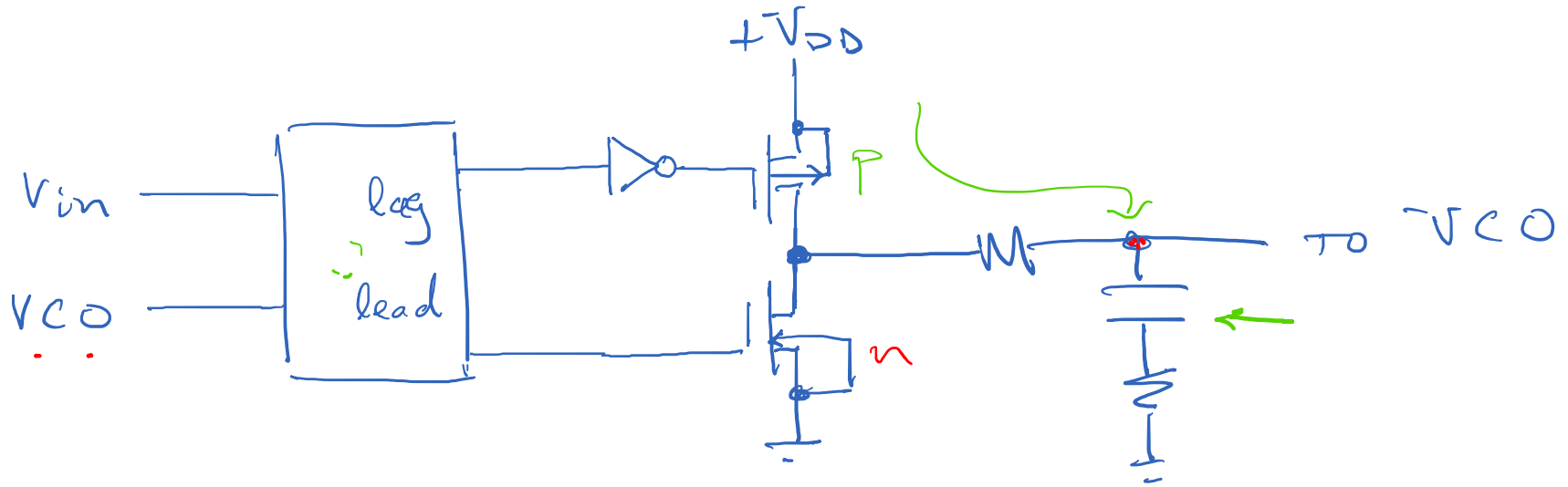
TYPE II P.D. [EDGE-SENSITIVE]

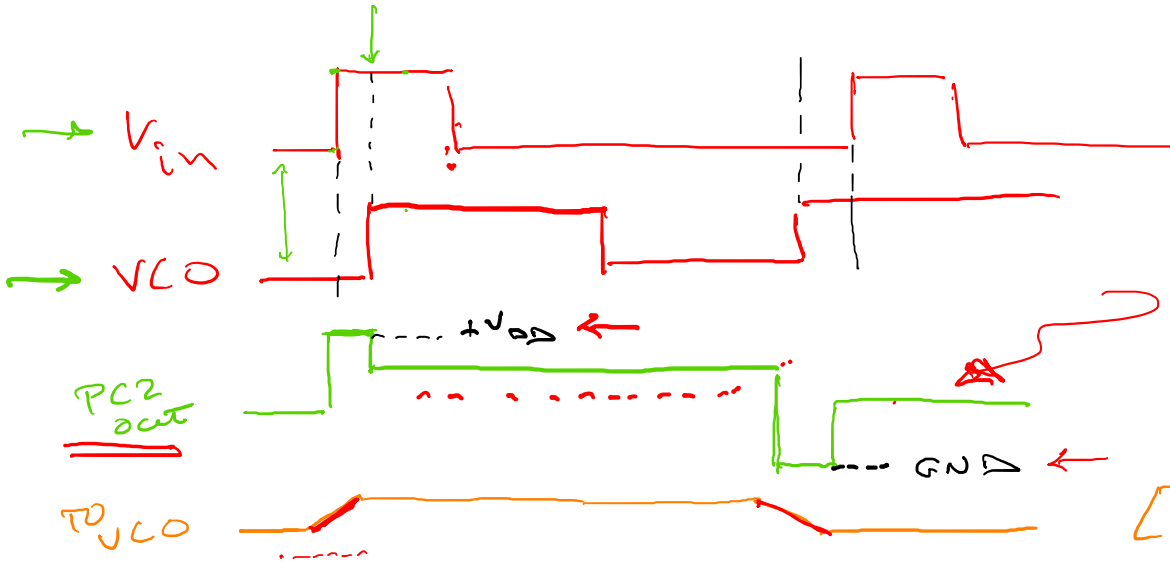
CMOS



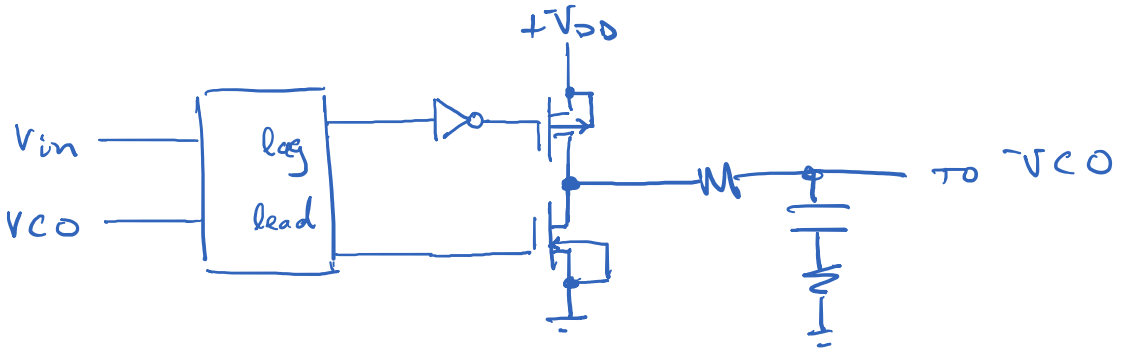
→ CHARGE/DISCHARGE CAP DEPENDING ON WHETHER INPUT LEADS/LAGS VCO

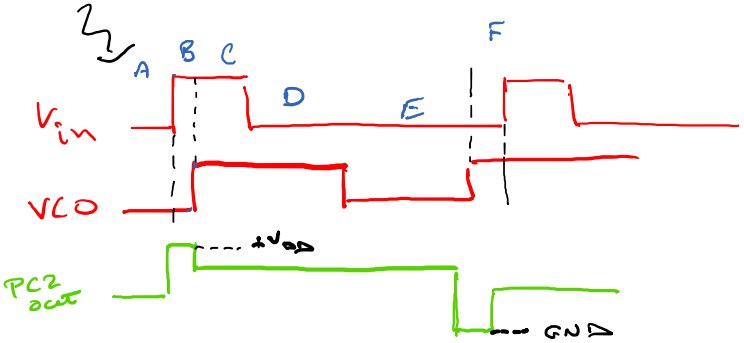
INTERNAL DIGITAL LOGIC ("STATE MACHINE")



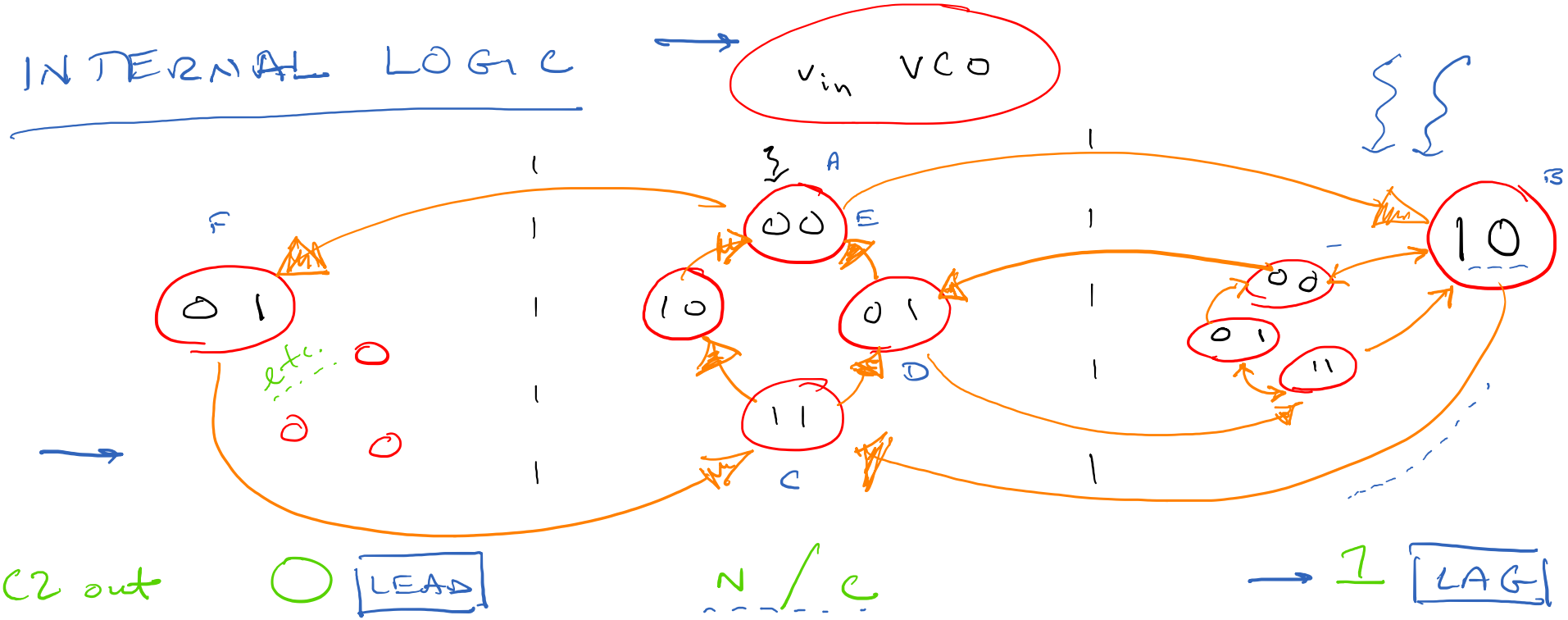


[CONST. $\frac{dV}{dt}$ FROM CURRENT SOURCE]





INTERNAL LOGIC

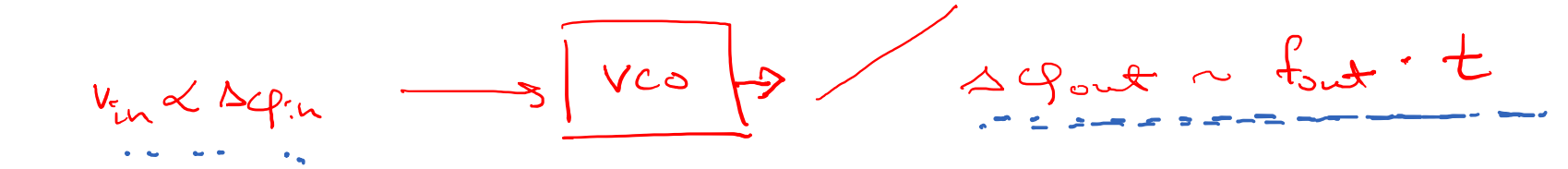


Phase Detector Comparison

	Type I	Type II
Input Duty Cycle	50%	Irrelevant
Lock on Harmonic?	Yes	No
Noise Rejection	Good	Poor
Ripple @ $2f_{in}$	High	Low
Capture Range	$f_c \leq f_{lock}$	$f_c = f_{lock}$

LOOP STABILITY

KEY POINT: VCO INTEGRATES PHASE ERROR



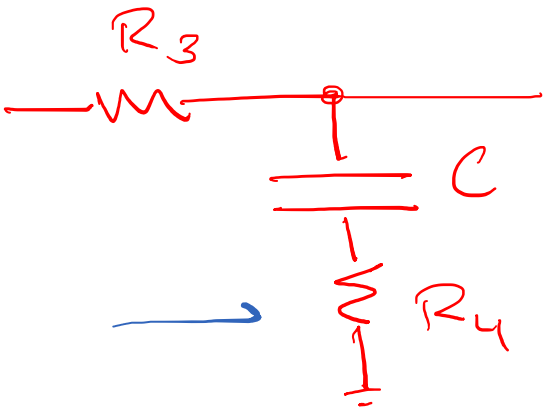
→ LIKE A SINGLE-POLE RC LOW-PASS / INTEGRATOR

→ INHERENT 90° DEG. PHASE SHIFT [FACTOR $\frac{1}{j\omega}$]

LOOP GAIN:

K_P (VOLTS/RAD) · K_F (DIM. LESS) · K_{VCO} (RAD/S / VOLT) · $\frac{1}{j\omega}$ ←

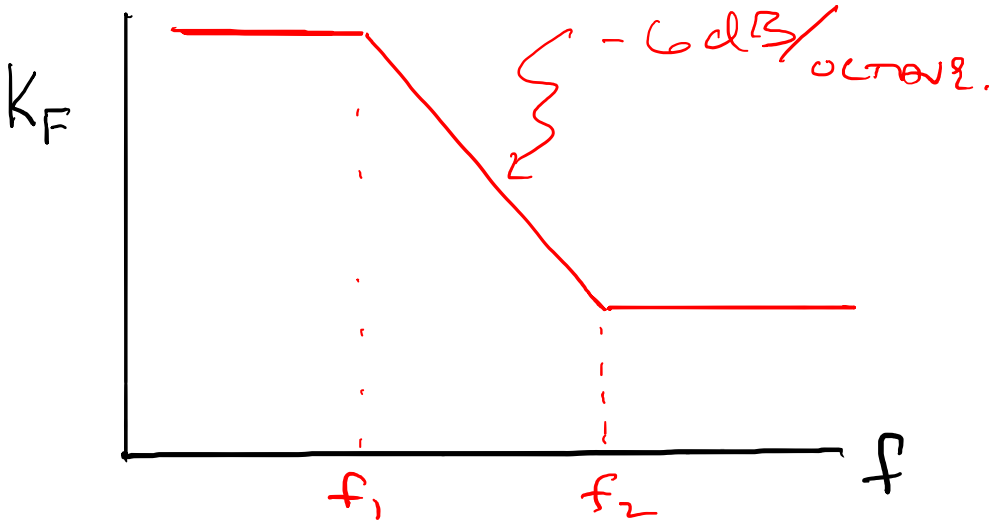
DESIGN OF FILTER?



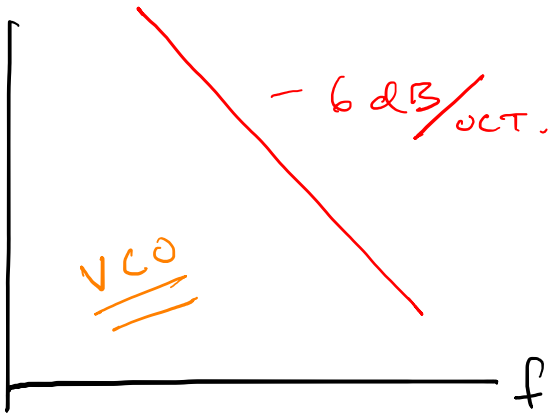
$$\frac{1}{R_3 C} \rightarrow \text{"POLE"}$$

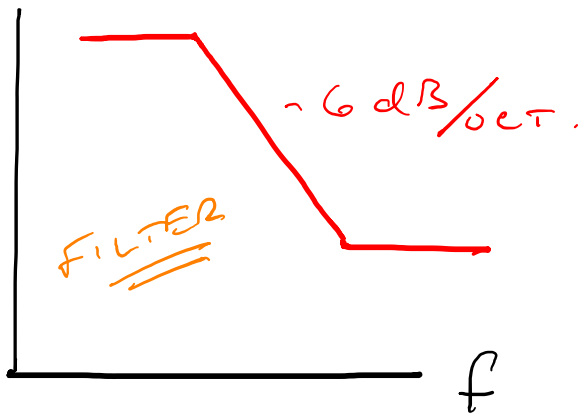
$$\frac{1}{R_4 C} \rightarrow \text{"ZERO"}$$

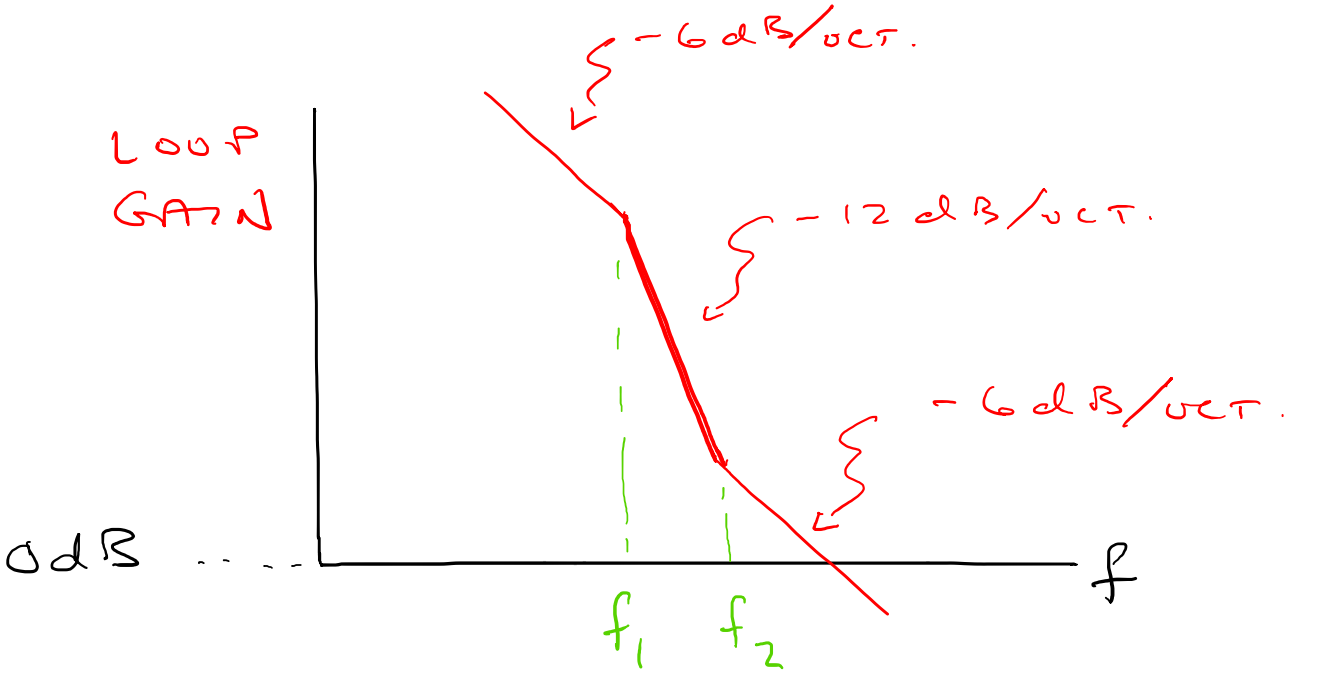
$$K_F = \frac{1 + j\omega R_4 C}{1 + j\omega (R_3 C + R_4 C)}$$



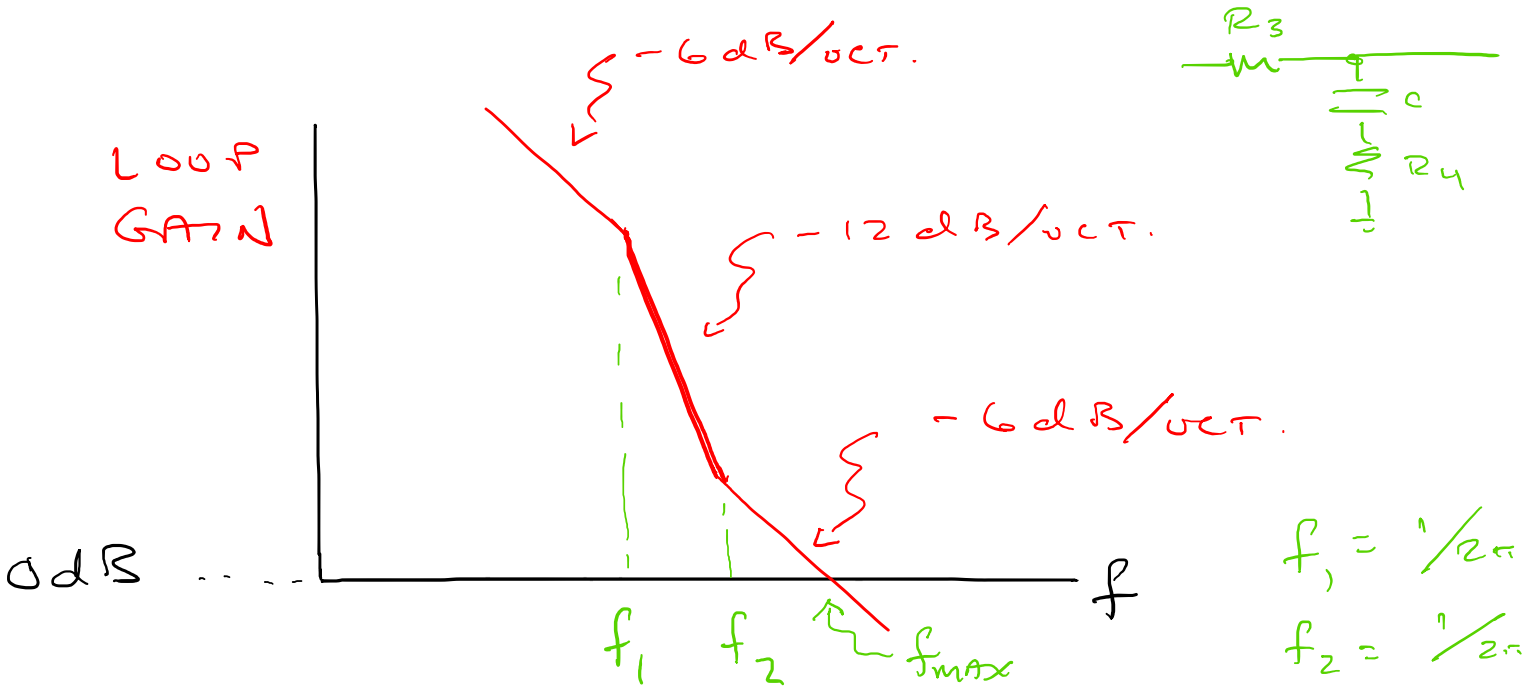
BODE


- 6 dB/OCT.
VCO
f


- 6 dB/OCT.
FILTER
f


- 6 dB/OCT.
LOOP GAIN
- 12 dB/OCT.
- 6 dB/OCT.
0dB
f
f_1
f_2

BODE



$f_1 = 1/2\pi R_3 C$

$f_2 = 1/2\pi R_4 C$

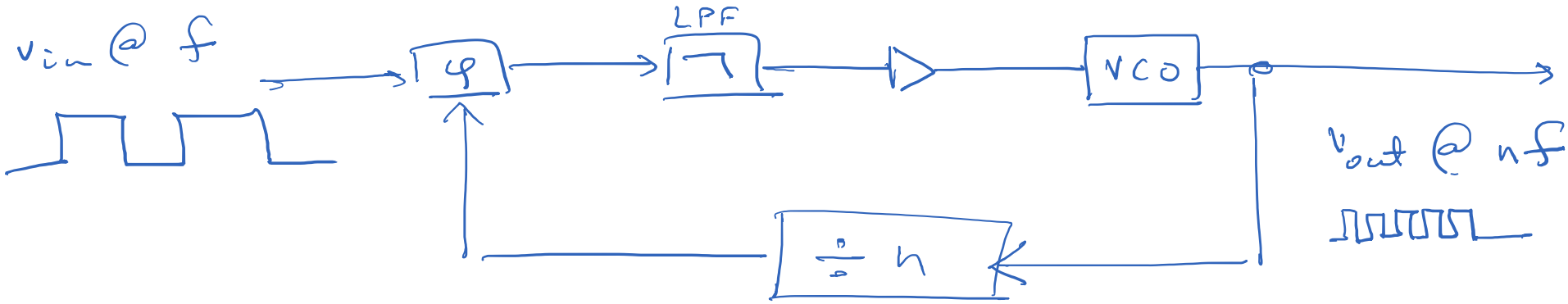
R_3C ⟶ SETS RESPONSE TIME OF PLL

⟶ PLL NEEDS TO BE FAST ENOUGH TO FOLLOW VARIATIONS OF INPUT SIGNAL, OTHERWISE LOWER FREQ. GIVES BETTER NOISE PERFORMANCE

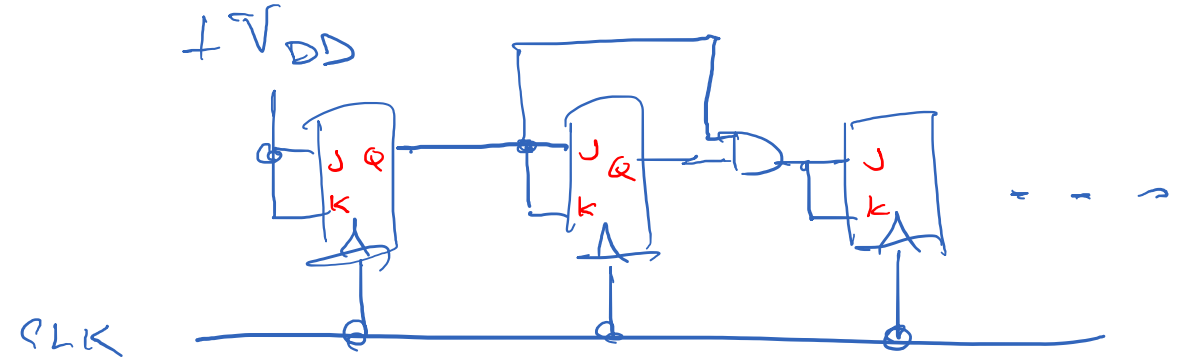
R_4/R_3 ⟶ DETERMINES DAMPING/OVERSHOOT TYP. $f_{MAX} = (3-5) \times f_2$

PLL APPLICATIONS

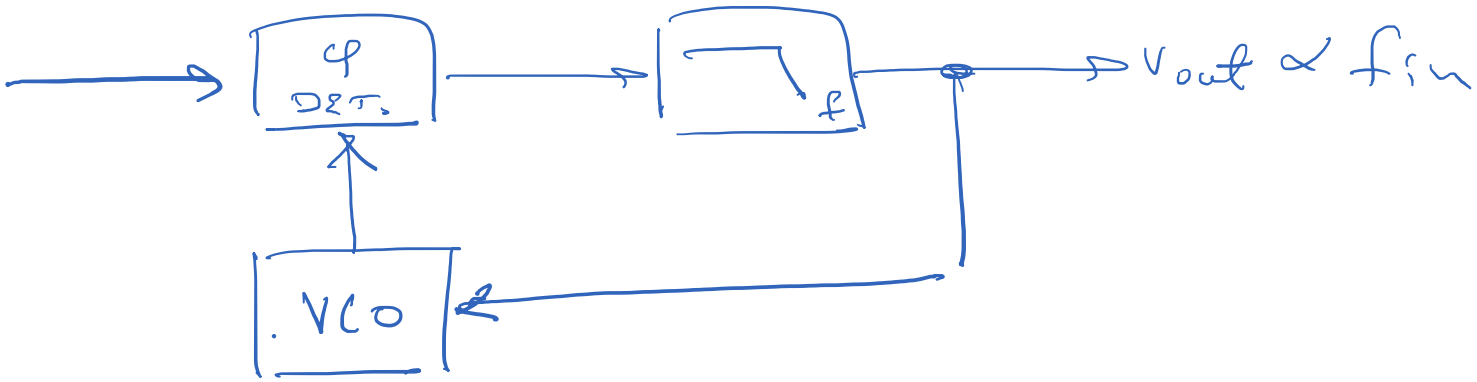
FREQUENCY MULTIPLICATION



e.g.



FM DEMODULATION



AM DETECTION
[HOMODYNE]