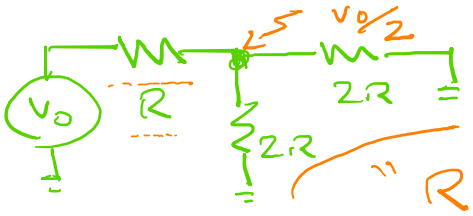
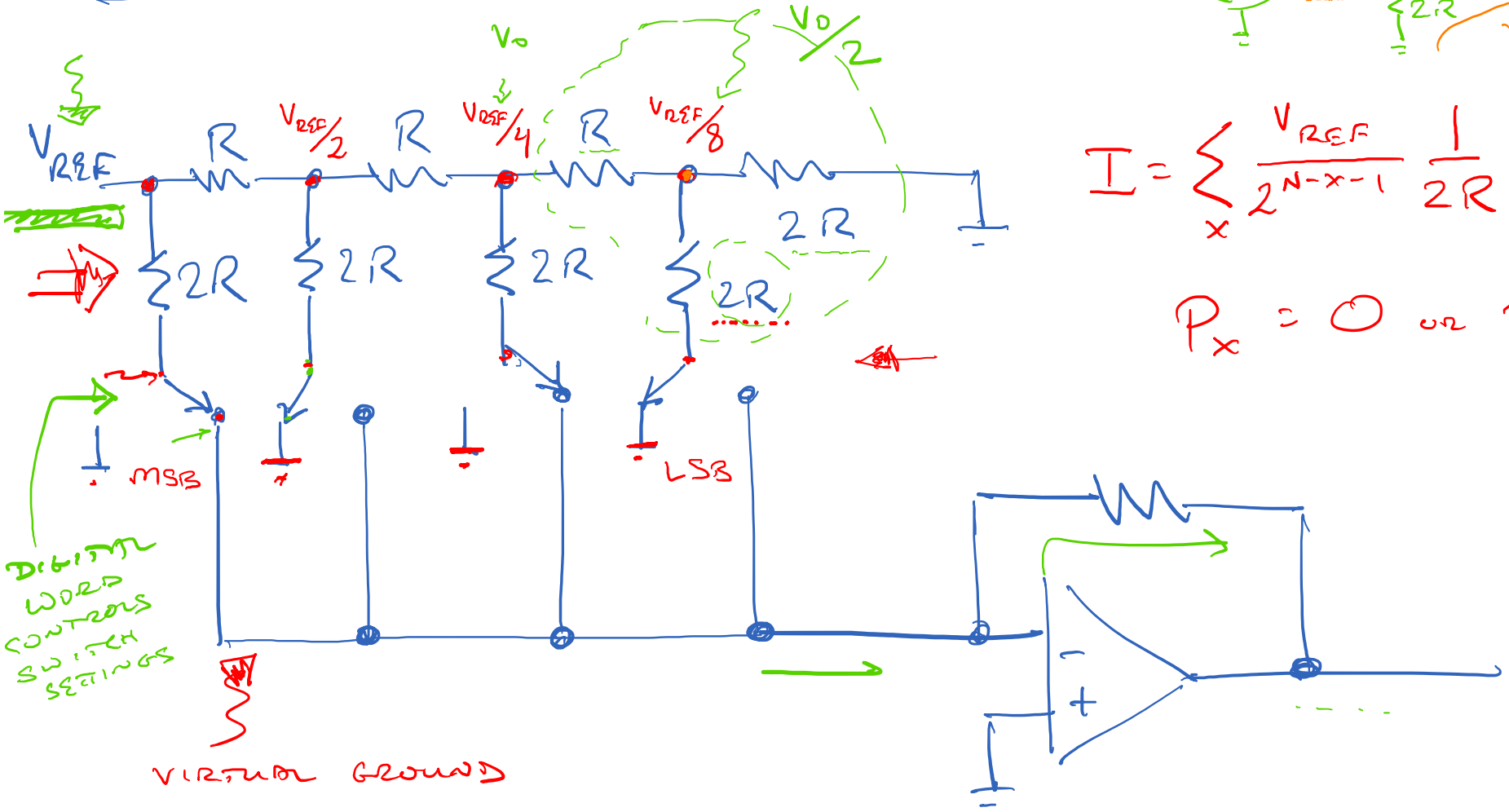
BETTER : R/2R LADDER





$$I = \sum_x \frac{V_{REF}}{2^{N-x-1}} \frac{1}{2R} P_x ;$$

$$P_x = 0 \text{ or } 1$$

AD CONVERSION

e.g. AUDIO ~20 Hz → 20 kHz

CD: 44 kHz SAMPLING RATE

2 × 16 BIT CHANNELS [~ 1:65K RESOLUTION]

MP3: 16 kHz SAMPLING RATE

8 BIT CHANNEL 1:256 RESOLUTION

→ TRADEOFF IN ADC: SPEED vs RESOLUTION

BANDWIDTH

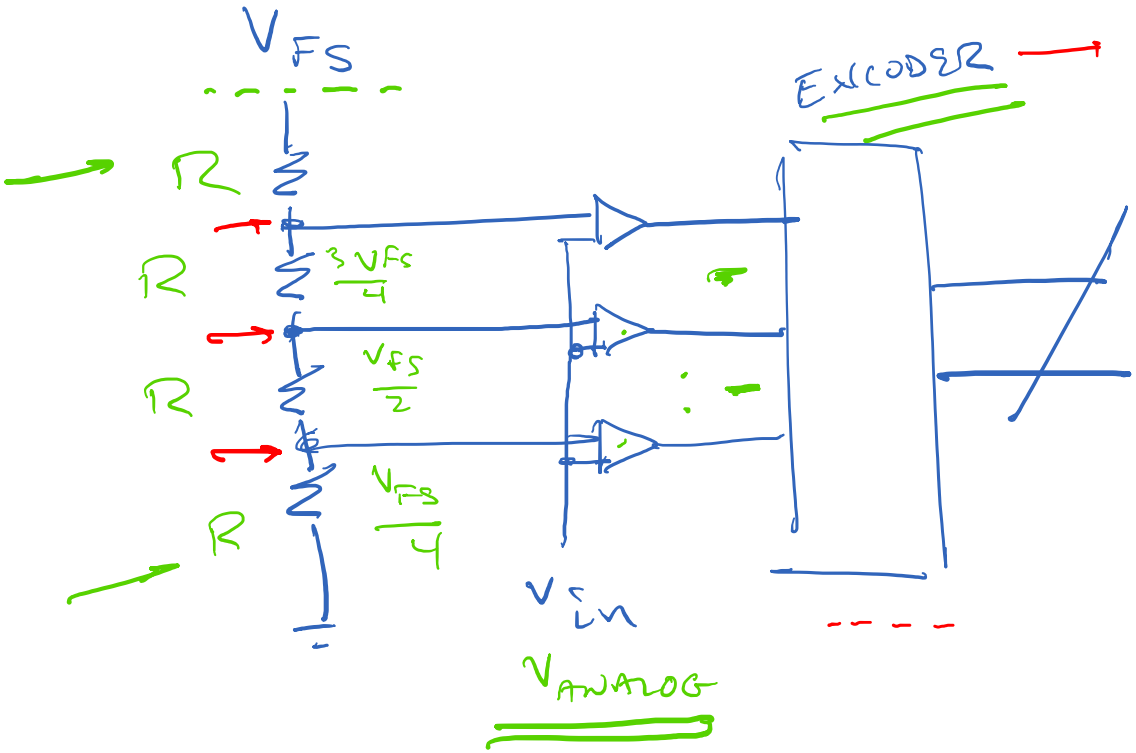
DYNAMIC RANGE

OTHER CONSIDERATIONS: LINEARITY, ABSOLUTE ACCURACY, ETC.

FAST : PARALLEL ENCODING / FLASH ADC

n BITS : DIVIDE V_{FS} INTO 2^n EQUAL INTERVALS

[REQ. $2^n - 1$ COMPARATORS]



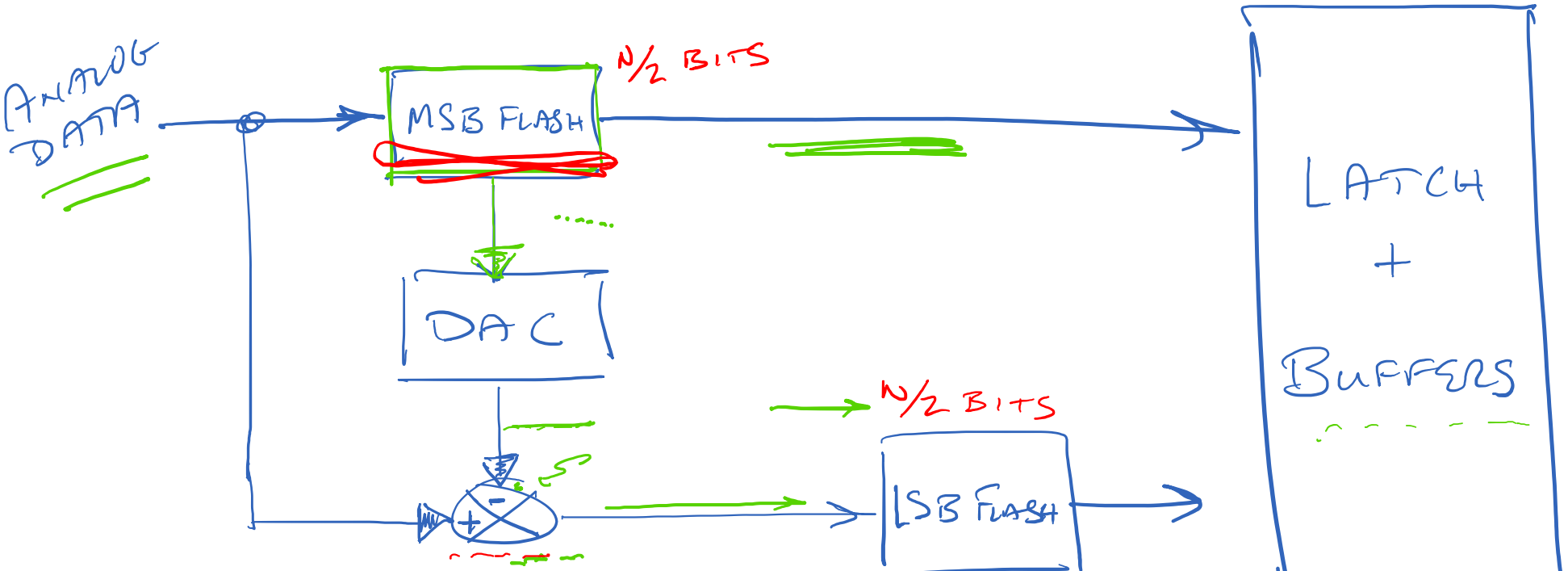
RETURN BINARY ADDRESS OF HIGHEST COMPARATOR THAT IS ASSERTED

2 BIT OUTPUT

~ 20 ns PROPAGATION DELAY [COMPARATORS + ENCODER]

HIGHER RESOLUTION, SLIGHTLY SLOWER:

"½ FLASH"

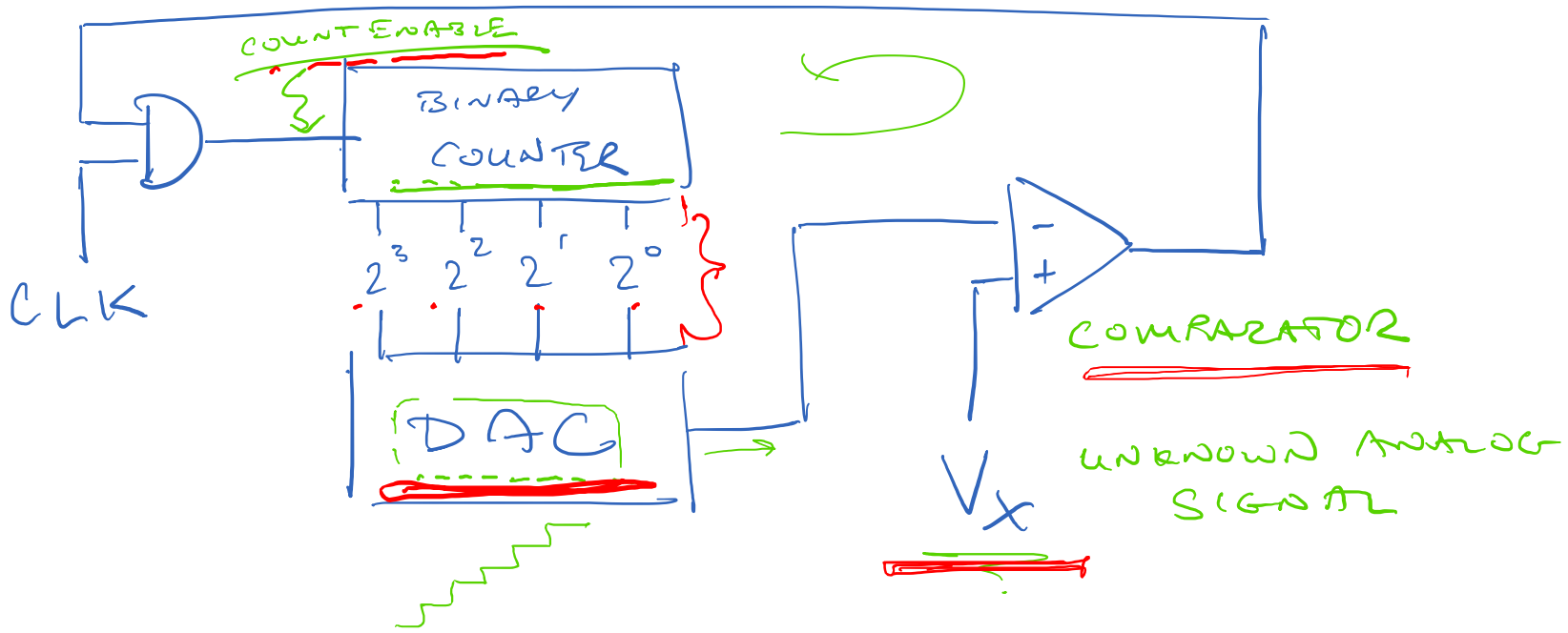


$[2^{N/2} - 1] \times 2$ COMPARATORS $\approx 2^{(\frac{N}{2}+1)}$

$\approx$ ½ AS FAST AS FULL FLASH

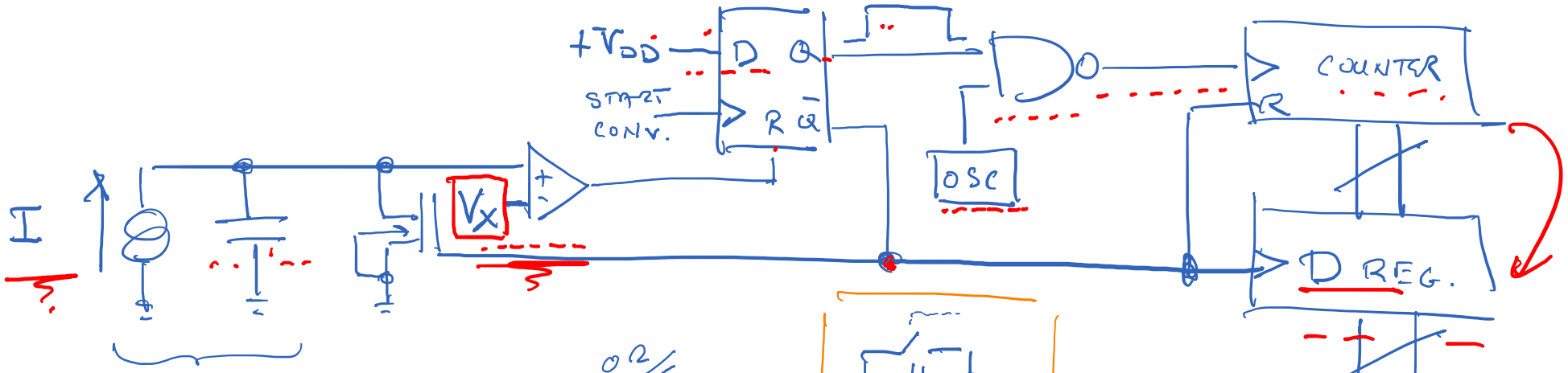
IN LAB: SIMPLE ADC BASED ON

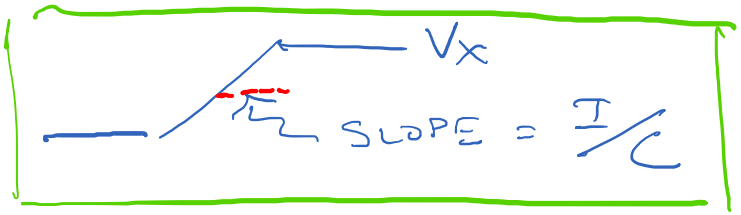
BINARY COUNTER + DAC IN FEEDBACK LOOP



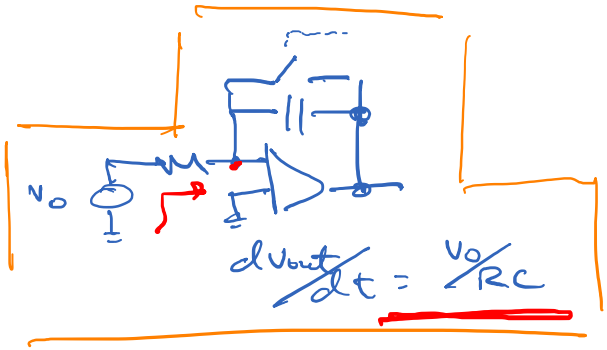
VARIANT OF SINGLE-SLOPE ADC

SINGLE SLOPE ADC





OR



→ USE COMPARATOR TO STOP BINARY COUNTER THAT IS CLOCKED @ FREQUENCY f_0

FOR INPUT VOLTAGE V_x,

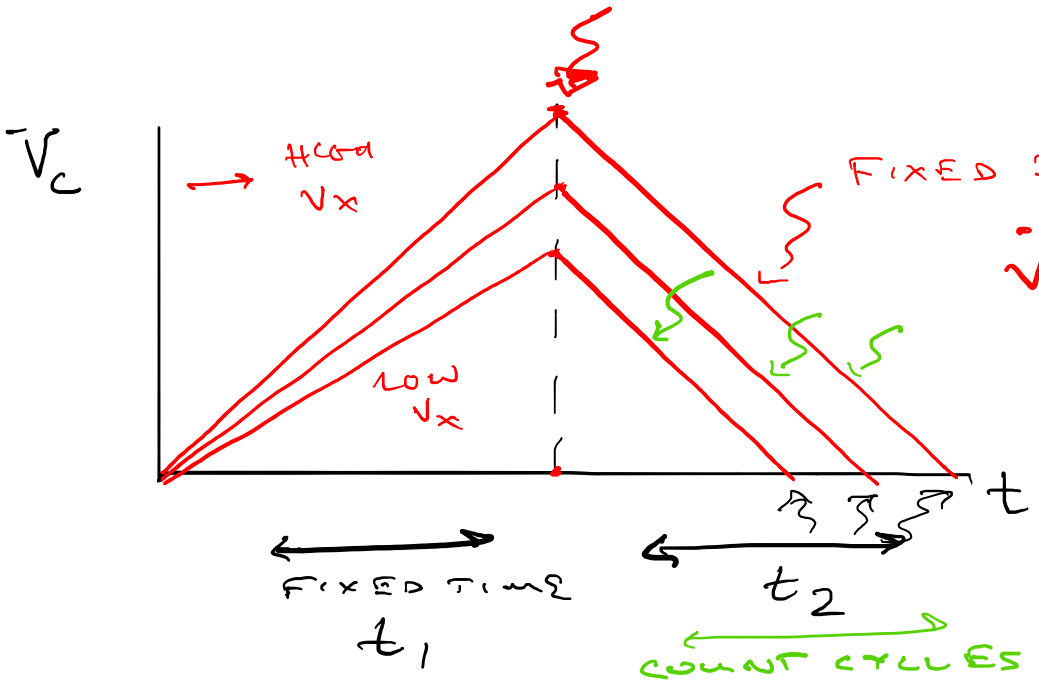
$$N_x = f_0 \Delta t = f_0 RC \, V_x/V_0$$

N_x → DIGITAL REPRESENTATION OF V_x

→ STRICT DEMANDS ON FREQUENCY STABILITY, ACCURACY OF CAP & COMPARATOR

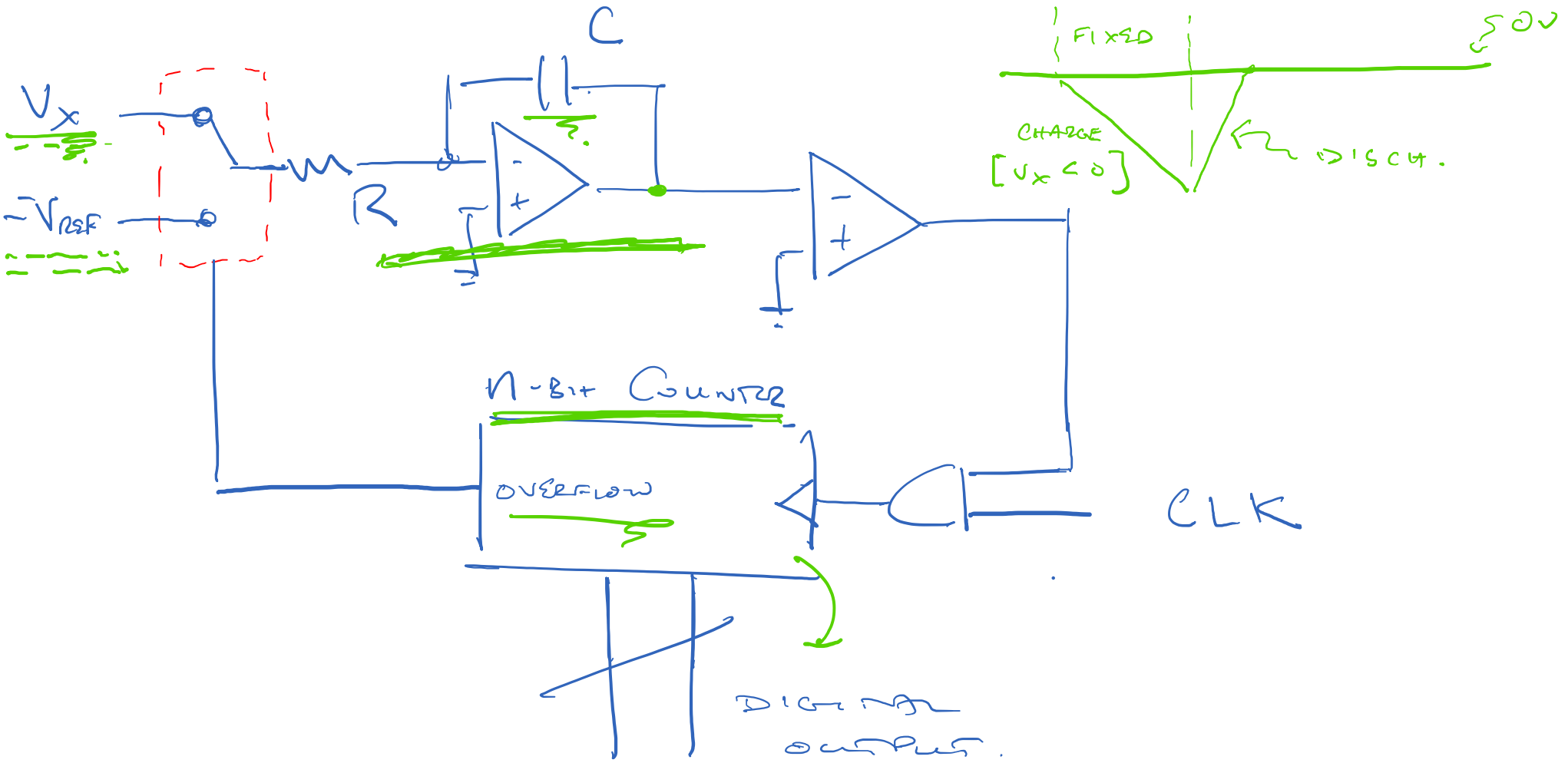
BETTER: DUAL SLOPE ADC

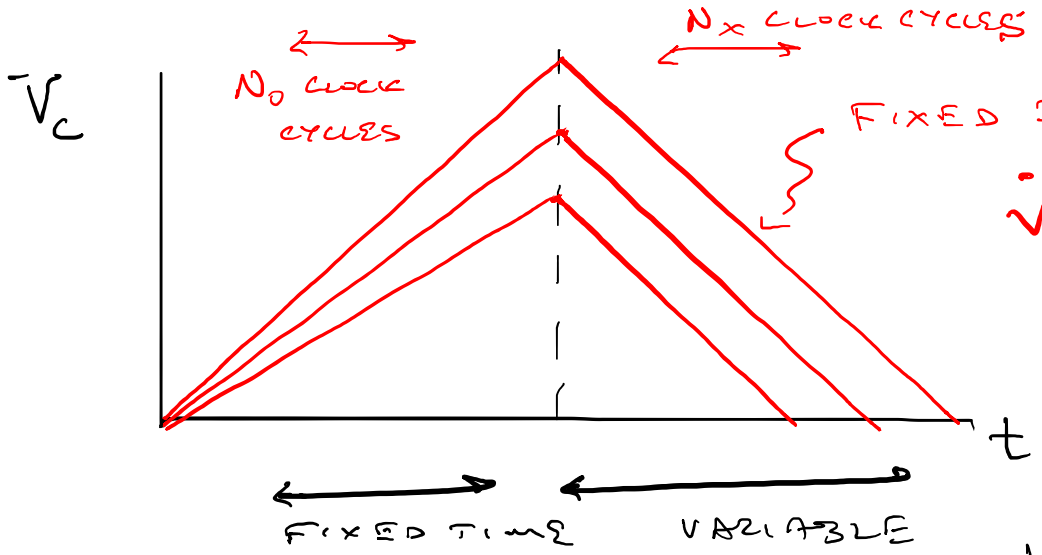
1. CHARGE CAP FOR FIXED TIME @ RATE PROPORTIONAL TO ANALOG INPUT VOLTAGE
2. THEN DISCHARGE CAP ALL THE WAY TO ZERO @ FIXED CURRENT



FIXED DISCHARGE CURRENT

$$\dot{V}_c = S_{DISCH} = I/C$$


C
FIXED
5V
V_x
$-V_{REF}$
R
CHARGE
$[V_x < 0]$
DISCH.
N-Bit COUNTER
OVERFLOW
CLK
DIGITAL
OUTPUT.



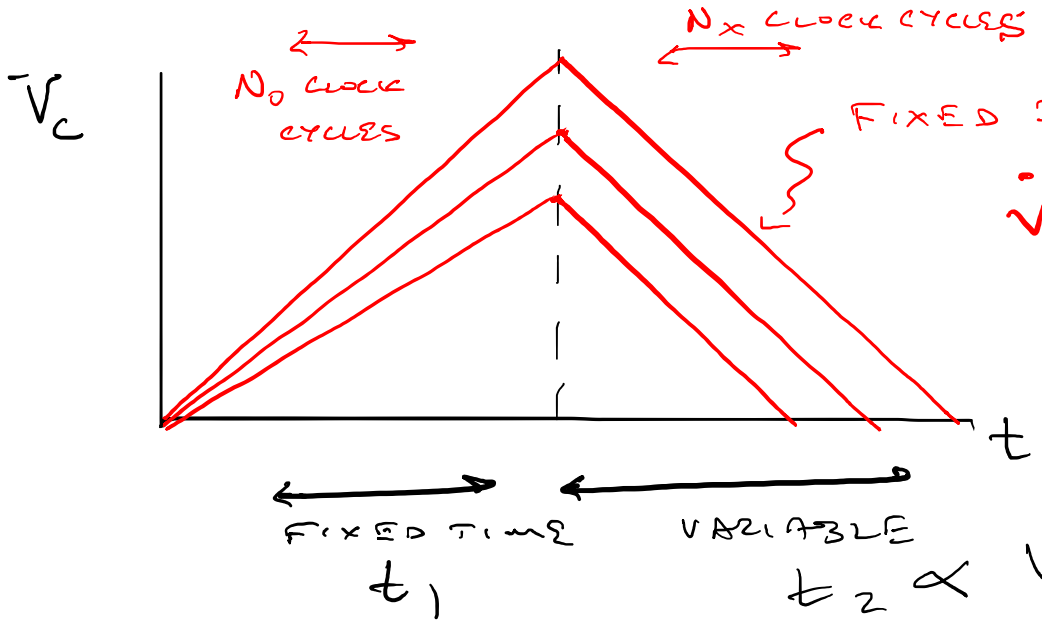
t_1

$t_2 \propto V_x$

$$t_2 = \frac{V_c(t_1)}{S_{DISCH}} = \frac{S_{CHARGE} \cdot t_1}{S_{DISCH}} \quad \Rightarrow \quad S_{CHARGE} = \frac{V_x}{RC}, \quad S_{DISCH} = \frac{V_{REF}}{RC}$$

$$t_2 = \frac{V_x}{V_{REF}} \cdot t_1 = \frac{V_x}{V_{REF}} \frac{N_0}{f_0} \Rightarrow \boxed{N_x = \frac{V_x}{V_{REF}} \cdot N_0}$$

→ NO EXPLICIT DEPENDENCE ON f_0, C



$$\dot{V}_C = S_{DISCH} = I/C$$

$$N_x = \frac{V_x}{V_{REF}} \cdot N_0$$

* CHOOSE CHARGING INTERVAL TO BE INTEGER MULTIPLE OF 60 Hz PERIOD
  → INSENSITIVITY TO LINE INTERFERENCE

PRECISE BUT SLOW

Application of Single/Dual Slope ADC's

→ Pulse Height Analyzer

→ ADC followed by multichannel scaler [counter]

→ input V_x [pulse height, ∝ energy of incident radiation]

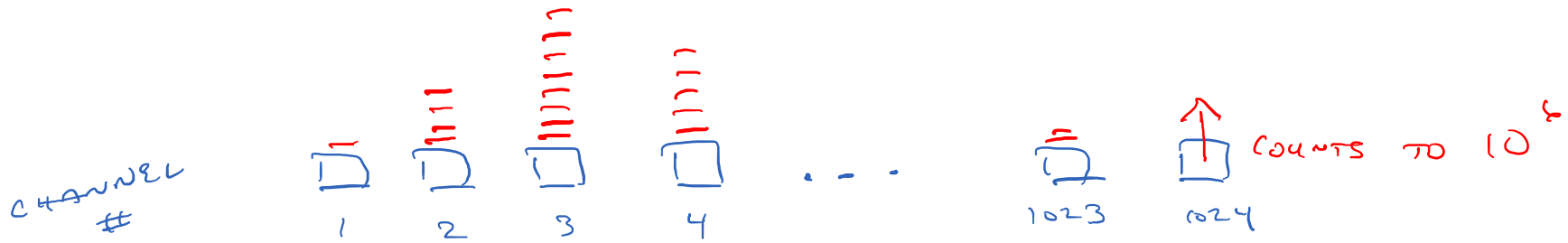
→ produce a binary address via the ADC

$V_x \rightarrow N_x$ [address of a particular scaler/counter]

e.g., 10 bit ADC → 2^{10} channels/scalers

Each scaler involves N-bit counter, e.g. N = 20

$2^{20} \sim 10^6$



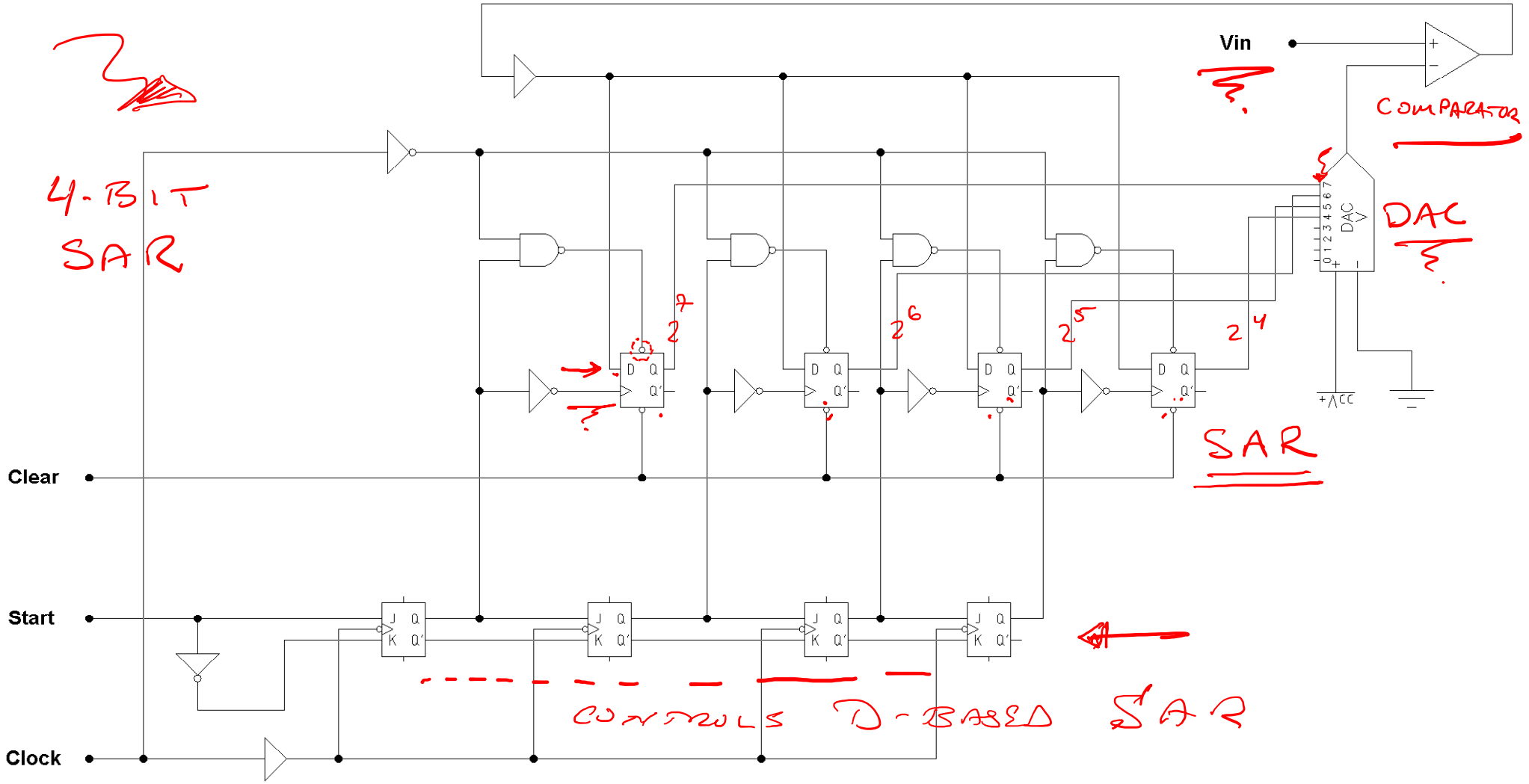
Successive Approximation ADC

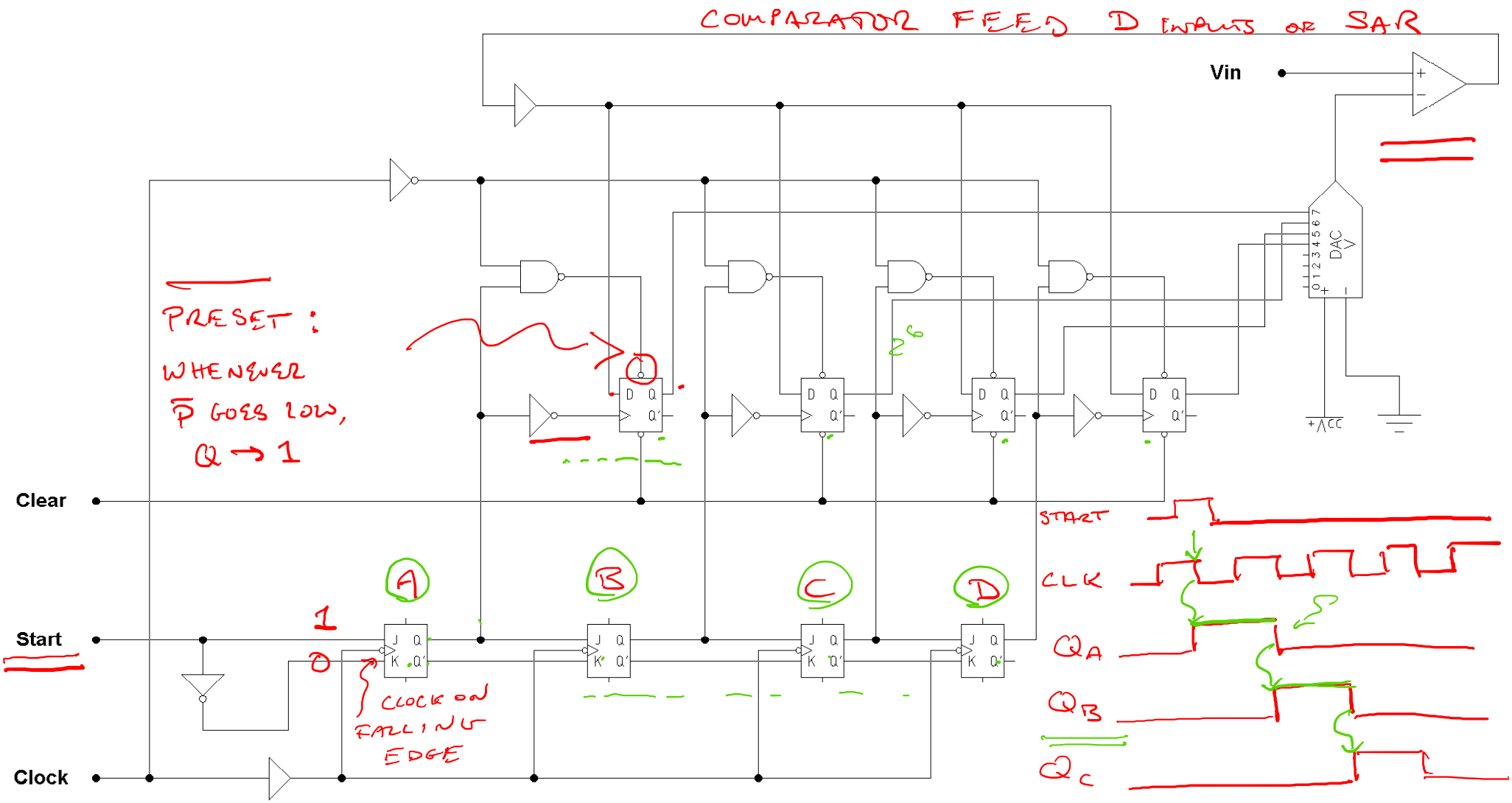
→ moderately fast, moderately hi-res.

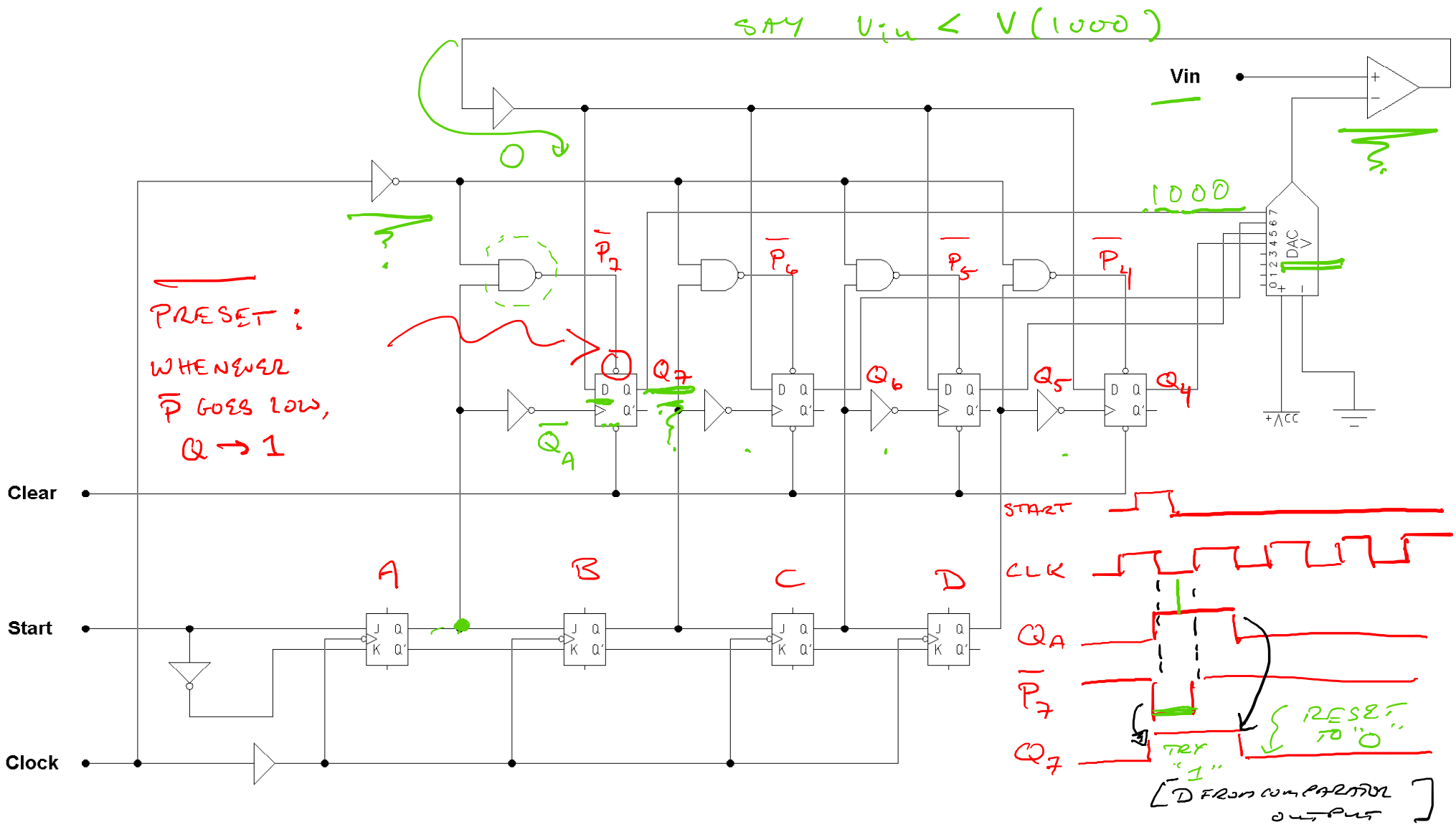
1. Set each bit of a DAC in turn & compare DAC output to V_x w/ comparator
2. If $V_x > V_{DAC}$, keep the bit & set next most sig. bit
3. If $V_x < V_{DAC}$, set the bit to 0 & set next most sig. bit

Etc. //

N bits requires N steps [8-12 bits: 1-50 μs]


4-BIT
SAR
Vin
COMPARATOR
DAC
SAR
Clear
Start
Clock
CONTROLS D-BASED SAR


COMPARATOR FEED D INPUTS OF SAR
Vin
DAC
PRESET :
WHENEVER
$\overline{P}$ GOES LOW,
Q → 1
Clear
Start
Clock
A
B
C
D
1
0
CLOCK ON
FALLING
EDGE
START
CLK
Q_A
Q_B
Q_C

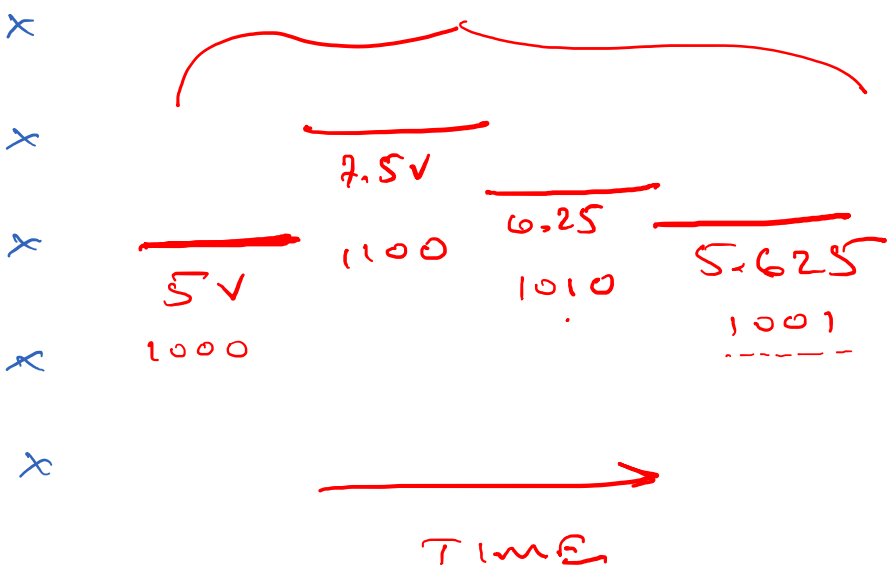

SAY Vin < V(1000)
Vin
1000
PRESET :
WHENEVER
$\overline{P}$ GOES LOW,
Q → 1
$\overline{P_7}$
$\overline{P_6}$
$\overline{P_5}$
$\overline{P_4}$
Q_7
Q_6
Q_5
Q_4
Q_A
DAC
+VCC
Clear
Start
Clock
A
B
C
D
START
CLK
Q_A
$\overline{P_7}$
Q_7
RESET TO "0"
TRY "1"
[D FROM COMPARATOR OUTPUT]

e.g. FS = 10 V

43.75

2^3	2^2	2^1	2^0
$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$ × FS
5 V	2.5 V	1.25 V	0.625 V

$V_x = 6$ V → DAC output from SAR



$V_D = 5.625$ V

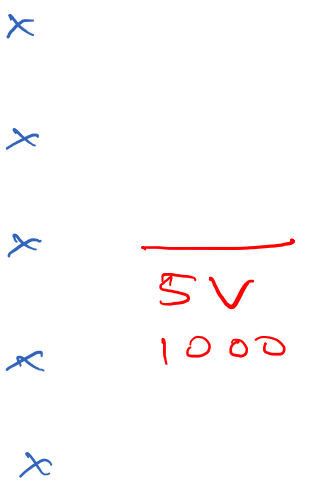
1001

e.g. FS = 10 V

4 B, T S

2^3	2^2	2^1	2^0	
$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\times$ FS
5 V	2.5 V	1.25 V	0.625 V	

$V_x = 8$ V



8.75 — 8.125 $\Rightarrow V_D = 7.5$ V

7.5

1110 1101

1100

5 V

1000

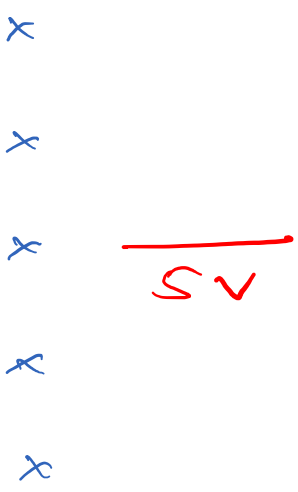
1100

e.g. FS = 10 V

4 B, 7 S

2^3	2^2	2^1	2^0	
$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	× FS
5 V	2.5 V	1.25 V	0.625 V	

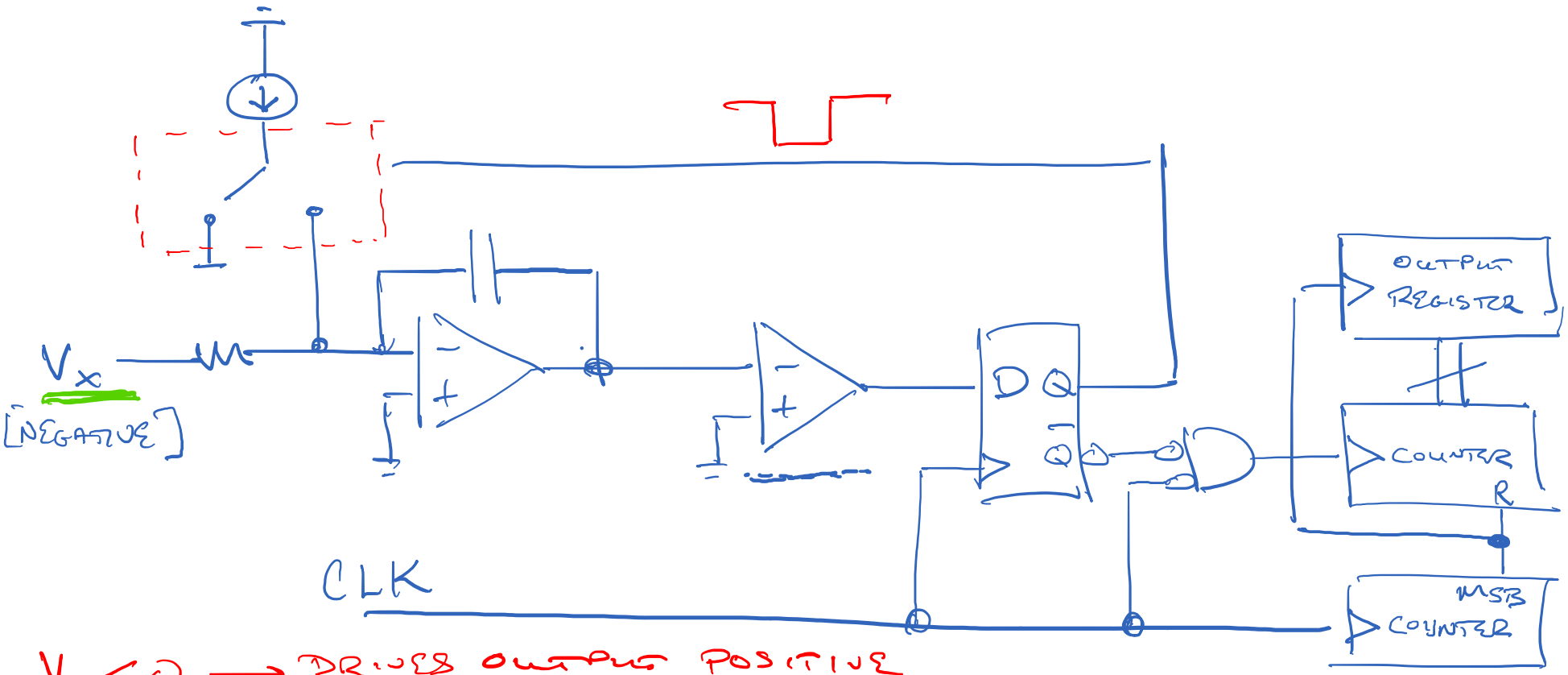
$V_x = 0.8\,V$



$V_D = 0.625\,V$

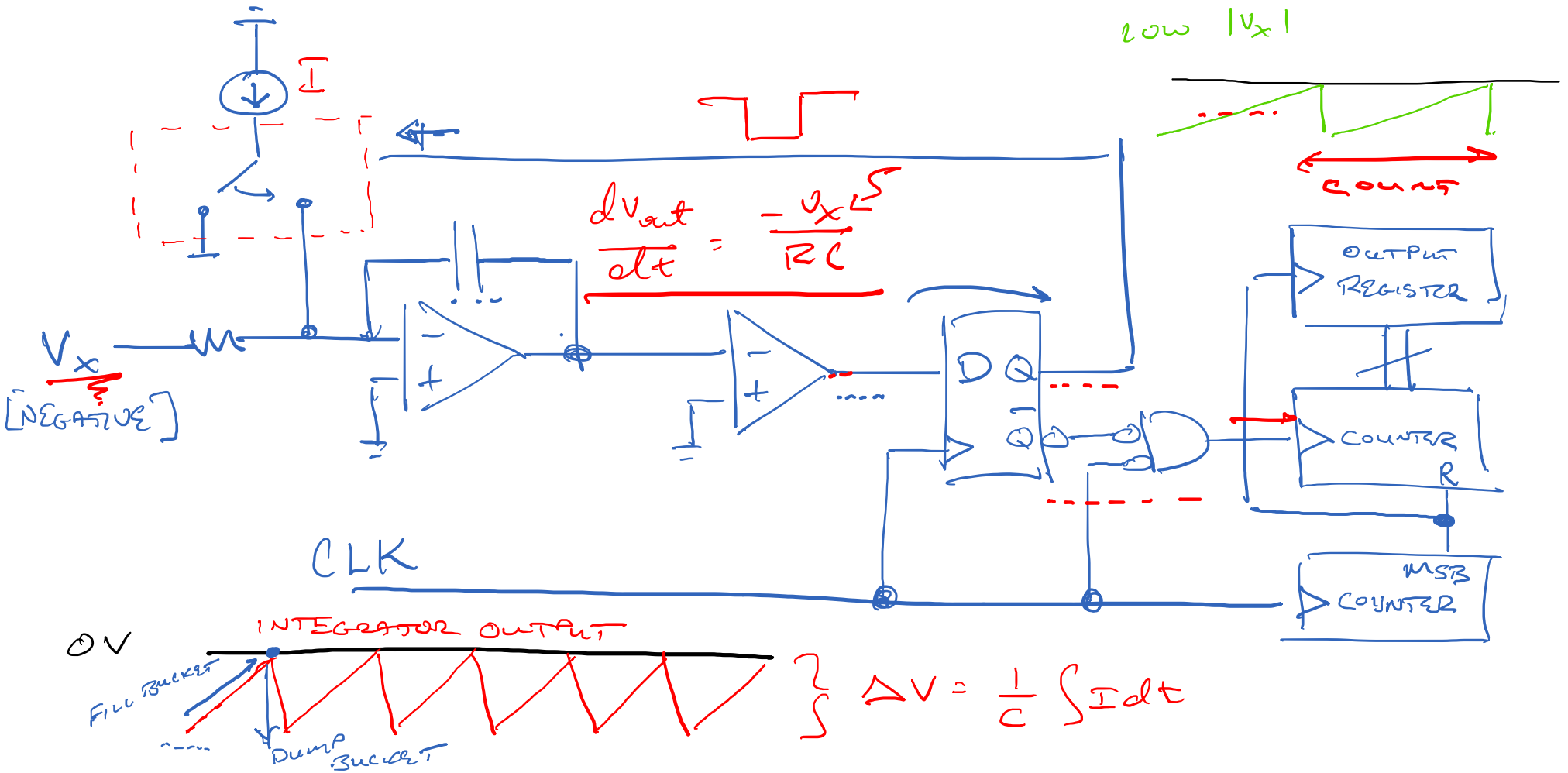
$\Rightarrow$ 0001

CHARGE-BALANCING ADC : Δ-Σ

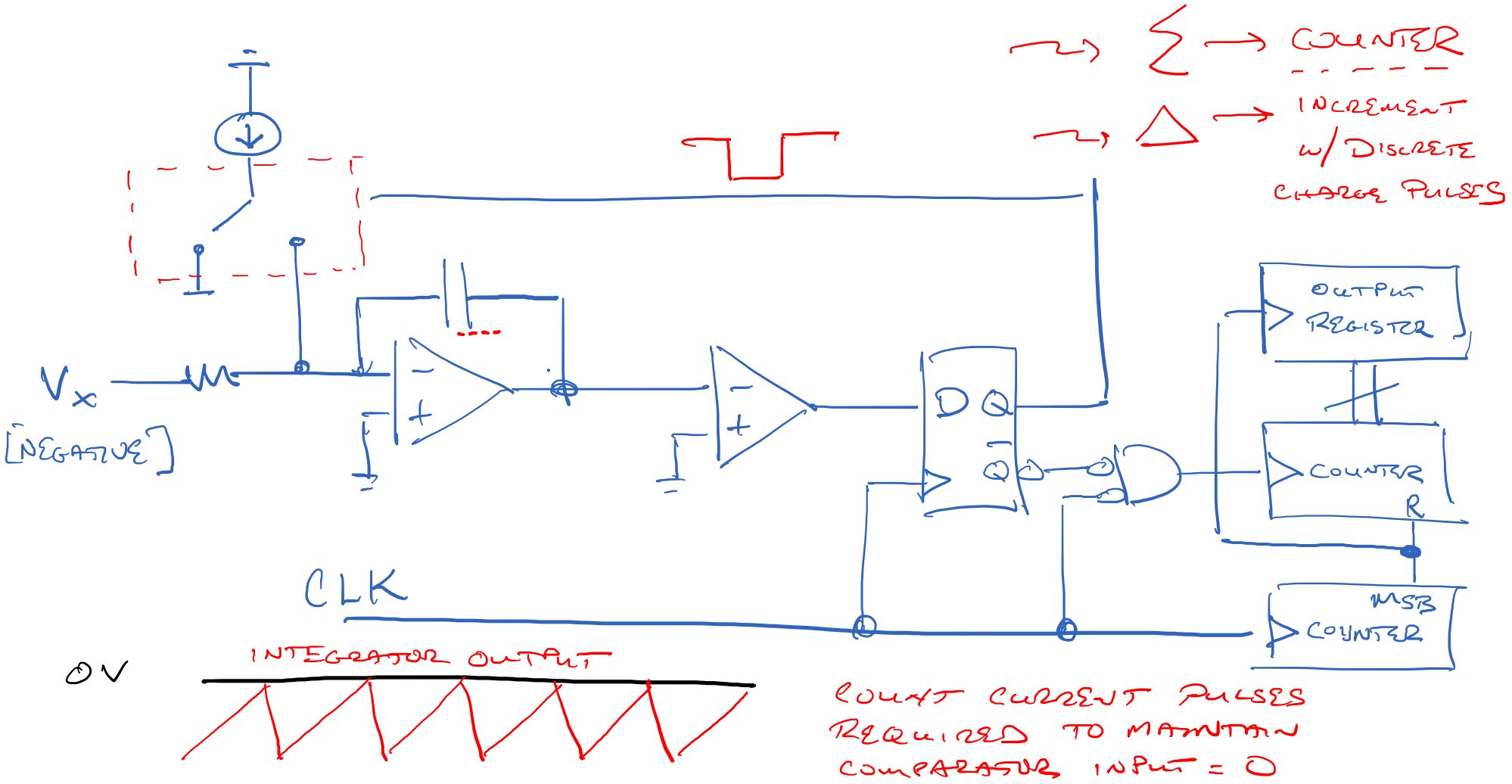


$V_x < 0$ → DRIVES OUTPUT POSITIVE
DRIVES COMPARATOR NEGATIVE
THIS CAUSES Q → 0 [INJECT CHARGE BALANCING PULSE]

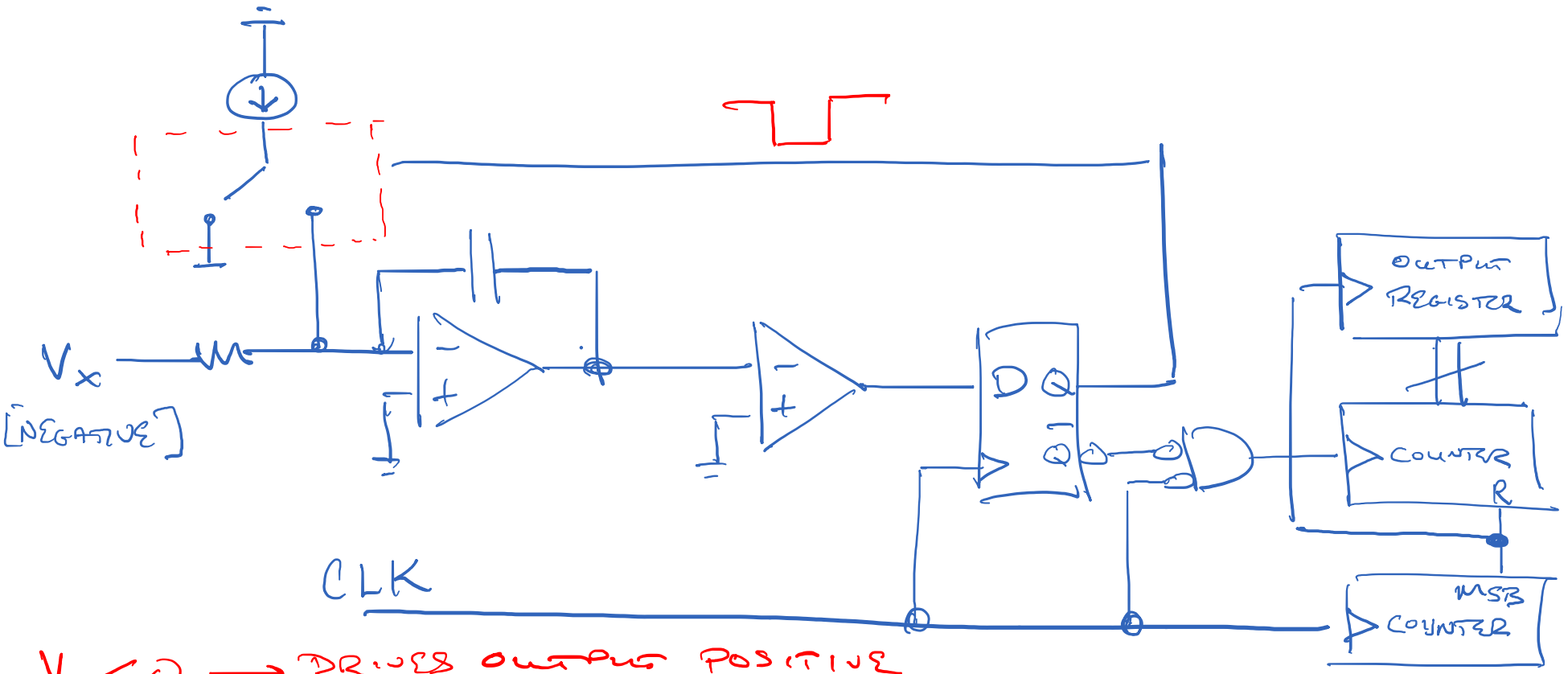
CHARGE-BALANCING ADC : Δ-Σ



CHARGE-BALANCING ADC : Δ-Σ



CHARGE-BALANCING ADC : Δ-Σ



$V_x < 0$ → DRIVES OUTPUT POSITIVE
DRIVES COMPARATOR NEGATIVE
THIS CAUSES Q → 0 [INJECT CHARGE BALANCING PULSE]

SUMMARY

	SPEED	RESOLUTION
→ FLASH	FAST [~20ns]	POOR [→ ~10 BIT]
→ SINGLE/DUAL SLOPE	SLOW [~ ms]	EXCELLENT [~24 BIT]
SAR	MEDIUM [~ μs]	MODERATE [~16-20 BITS]
ΔΣ	MEDIUM [1-10 μs]	MODERATE [~16-20 BITS]