Physics 623 Homework 9

1. Design a dividy-by-3 circuit. Use the general "state machine" approach, where a minimum number of 'D' flip/flops "remember" the state. How many f/fs are required to distinguish three states?

a) Make a state diagram showing three states and how the machine should progress from each one whenever there is an input (clock) pulse. The output pulse can be taken from any of the three states.

b) Each input pulse clocks all the f/fs to go to the next state.

c) Make a Truth Table that shows what the D inputs should be for each state of the machine as represented by the Q outputs.

d) Implement this truth table with gates and show the complete schematic.

e) Check that if the machine is in an "illegal" state on power up, it will get out of it in a finite number of clock pulses.

2. Design a "reaction timer." It should have one pushbutton to be pressed by the operator. This immeditately lights an LED (light-emitting diode) and starts a timer. The testee has a button they press as soon as they see the LED come on. This stops the timer and displays the elapsed time in milliseconds on a 3-digit base-10 display that uses three 7-segment LED display units. A third pushbutton resets the display to zero.

You could use a set/reset flip-flop for the start and stop function. You have 74LS192 counter chips (these share the 74LS193 data sheet you can find on the course webpage), a 1 kHz crystal clock that puts out one positive-going pulse every millisecond, push button switches, and any other logic gates and flip-flops you need. The 74192 differs from the 74193 in that it has internal feedback so it resets to zero on the tenth input pulse. So if you cascade three of these, you get what is called "binary-coded decimal" output. For each digit, you have to decode the four binary bits to the digits zero through nine, but then you can just do the same thing on the next counter and the next, and you get a 3-digit decimal number. You can use three TIL-311 display chips (which combine a 7-segment display with binary decoder logic that decides which of the seven segments need to be on for binary inputs 0-9. You could make up a truth table for this — or look up the data sheet for a SN7446 BCD-to-7-segment decoder).

3. Detector A puts out 1 μs wide pulses with an average rate of about 100 Hz and a seemingly random distribution. the output of detector B looks similar when viewed by itself. We would like to find out how many of the events for the two detectors are actually correlated in a particular way. Use monostalbe multivibrators ("one-shots" of the 74LS221 variety), J-K flip-flops, counters, displays, and any logic gates you need to design a circuit which will determine how often an event occurs in detector B within 25 microseconds after an event in detector A. (To count such occurrences for a known length of time, you can use a "time-base" clock which puts out a 10-second wide pulse each time the start button is pressed. Just draw this as an appropriately-labeled box -- you could design it as another project.

4.

Use NAND gates to form the following:

(a) $(A \cdot B) + (C \cdot D)$

(b) $(A+B) \cdot \overline{(C+D)}$

(c) $A + (B \cdot \overline{C})$