



Improved, SPST/SPDT Analog Switches

DG417/DG418/DG419

General Description

Maxim's redesigned DG417/DG418/DG419 precision, CMOS, monolithic analog switches now feature guaranteed on-resistance matching (3Ω max) between switches and guaranteed on-resistance flatness over the signal range (4Ω max). These switches conduct equally well in either direction and guarantee low charge injection, low power consumption, and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers low off-leakage current over temperature (less than 5nA at +85°C).

The DG417/DG418 are single-pole/single-throw (SPST) switches. The DG417 is normally closed, and the DG418 is normally open. The DG419 is single-pole/double-throw (SPDT) with one normally closed switch and one normally open switch. Switching times are less than 175ns max for t_{ON} and less than 145ns max for t_{OFF} . Operation is from a single +10V to +30V supply, or bipolar $\pm 4.5V$ to $\pm 20V$ supplies. The improved DG417/DG418/DG419 are fabricated with a 44V silicon-gate process.

Applications

Sample-and-Hold Circuits	Communications Systems
Test Equipment	Battery-Operated Systems
Modems	Fax Machines
Guidance and Control Systems	PBX, PABX
Audio Signal Routing	Military Radios

New Features

- ◆ Plug-In Upgrades for Industry-Standard DG417/DG418/DG419
- ◆ Improved $R_{DS(ON)}$ Match Between Channels (3Ω max, DG419 only)
- ◆ Guaranteed $R_{FLAT(ON)}$ Over Signal Range (4Ω max)
- ◆ Improved Charge Injection ($10pC$ max)
- ◆ Improved Off-Leakage Current Over Temperature (<5nA at +85°C)
- ◆ Withstand Electrostatic Discharge (2000V min) per Method 3015.7

Existing Features

- ◆ Low $R_{DS(ON)}$ (35Ω max)
- ◆ Single-Supply Operation +10V to +30V
Bipolar-Supply Operation $\pm 4.5V$ to $\pm 20V$
- ◆ Low Power Consumption ($35\mu W$ max)
- ◆ Rail-to-Rail Signal Handling
- ◆ TTL/CMOS-Logic Compatible

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
DG417CJ	0°C to +70°C	8 Plastic DIP
DG417CY	0°C to +70°C	8 SO
DG417C/D	0°C to +70°C	Dice*
DG417DJ	-40°C to +85°C	8 Plastic DIP
DG417DY	-40°C to +85°C	8 SO

Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

DIP/SO

DG417	
LOGIC	SWITCH
0	ON
1	OFF

DIP/SO

DG418	
LOGIC	SWITCH
0	OFF
1	ON

DIP/SO

DG419		
LOGIC	SWITCH 1	SWITCH 2
0	ON	OFF
1	OFF	ON

N.C. = NO INTERNAL CONNECTION

SWITCHES SHOWN FOR LOGIC "0" INPUT

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ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+	44V
GND.....	25V
VL	(GND - 0.3V) to (V+ + 0.3V)
Digital Inputs V _S , V _D (Note 1)	(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) (Note 1)	30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) ..	100mA

Continuous Power Dissipation (T_A = +70°C)

Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
SO (derate 5.88mW/°C above +70°C)	471mW
CERDIP (derate 8.00mW/°C above +70°C)	640mW

Operating Temperature Ranges

DG41_C_	0°C to +70°C
DG41_D_	-40°C to +85°C
DG41_AK	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS		
SWITCH									
Analog Signal Range	V _S , V _D	(Note 3)		-15		15	V		
Drain-Source On-Resistance	R _{DS(ON)}	V+ = 13.5V, V- = -13.5V, V _D = ±10V, I _S = -10mA	T _A = +25°C	C, D	20	35	Ω		
				A	20	30			
			T _A = T _{MIN} to T _{MAX}			45			
On-Resistance Match Between Channels (Note 4)	ΔR _{DS(ON)}	V+ = 15V, V- = -15V, V _D = ±10V, I _S = -10mA	T _A = +25°C			3	Ω		
			T _A = T _{MIN} to T _{MAX}			4			
On-Resistance Flatness (Note 4)	R _{FLAT(ON)}	V+ = 15V, V- = -15V, V _D = ±5V, I _S = -10mA	T _A = +25°C			4	Ω		
			T _A = T _{MIN} to T _{MAX}			6			
Source-Off Leakage Current (Note 5)	I _{S(OFF)}	V+ = 16.5V, V- = -16.5V, V _D = ±15.5V, V _S = ±15.5V	T _A = +25°C		-0.25	0.25	nA		
			T _A = T _{MIN} to T _{MAX}	C, D	-5	5			
				A	-20	20			
Drain-Off Leakage Current (Note 5)	I _{D(OFF)}	V+ = 16.5V, V- = -16.5V, V _D = ±15.5V, V _S = ±15.5V	DG417/ DG418	T _A = +25°C		-0.25	0.1	nA	
				T _A = T _{MIN} to T _{MAX}	C, D	-5	5		
			DG419		T _A = +25°C		-0.75		-0.1
				T _A = T _{MIN} to T _{MAX}	C, D	-10	10		
			A		-40	40			
			Drain-On Leakage Current (Note 5)	I _{D(ON)}	V+ = 16.5V, V- = -16.5V, V _D = ±15.5V, V _S = ±15.5V	DG417/ DG418	T _A = +25°C		-0.4
T _A = T _{MIN} to T _{MAX}	C, D	-10					10		
	DG419	T _A = +25°C				-0.75	0.75		
T _A = T _{MIN} to T _{MAX}		C, D				-10	10		
	A	-40				40			

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ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, VINL = 0.8V, VINH = 2.4V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS	
LOGIC INPUT							
Logic Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V	-0.5	0.005	0.5	μA	
Logic Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V	-0.5	0.005	0.5	μA	
DYNAMIC							
Turn-On Time	t _{ON}	DG417/DG418, V _D = ±10V, Figure 2	TA = +25°C	100	175	ns	
			TA = T _{MIN} to T _{MAX}		250		
Turn-Off Time	t _{OFF}	DG417/DG418, V _D = ±10V, Figure 2	TA = +25°C	60	145	ns	
			TA = T _{MIN} to T _{MAX}		210		
Transition Time	t _{TRANS}	DG419, V _S = ±10V, Figure 3	TA = +25°C		175	ns	
			TA = T _{MIN} to T _{MAX}		250		
Break-Before-Make Interval	t _D	DG419, V _{S1} = V _{S2} = ±10V, Figure 4, TA = +25°C	5	13		ns	
Charge Injection (Note 3)	Q	V _{GEN} = 0V, Figure 5, TA = +25°C		3	10	pC	
Off-Isolation Rejection Ratio (Note 6)	OIRR	R _L = 500Ω, C _L = 5pF, f = 1MHz, Figure 6, TA = +25°C		68		dB	
Crosstalk (Note 7)		DG419, R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 7, TA = +25°C		85		dB	
Drain Off-Capacitance	C _{D (OFF)}	V _D = 0V, f = 1MHz, Figure 8, TA = +25°C		8		pF	
Source Off-Capacitance	C _{S (OFF)}	V _D = 0V, f = 1MHz, Figure 8, TA = +25°C		8		pF	
Drain-Source On-Capacitance	C _{D (ON)} or C _{S (ON)}	V _S = 0V, f = 1MHz, Figure 9, TA = +25°C	DG417/DG418	30		pF	
			DG419	35			
SUPPLY							
Positive Supply Current	I ₊	V ₊ = 16.5V, V ₋ = -16.5V, V _{IN} = 0V or 5V	TA = +25°C	-1	-0.0001	1	μA
			TA = T _{MIN} to T _{MAX}	-5		5	
Negative Supply Current	I ₋	V ₊ = 16.5V, V ₋ = -16.5V, V _{IN} = 0V or 5V	TA = +25°C	-1	-0.0001	1	μA
			TA = T _{MIN} to T _{MAX}	-5		5	
Logic Supply Current	I _L	V ₊ = 16.5V, V ₋ = -16.5V, V _{IN} = 0V or 5V	TA = +25°C	-1	-0.0001	1	μA
			TA = T _{MIN} to T _{MAX}	-5		5	
Ground Current	I _{GND}	V ₊ = 16.5V, V ₋ = -16.5V, V _{IN} = 0V or 5V	TA = +25°C	-1	-0.0001	1	μA
			TA = T _{MIN} to T _{MAX}	-5		5	

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ELECTRICAL CHARACTERISTICS—Single Supply

(V₊ = +12V, V₋ = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
SWITCH						
Analog Signal Range	V _{ANALOG}	(Note 3)	0		12	V
Drain-Source On-Resistance	R _{DS(ON)}	I _S = -10mA, V _D = 3.8V, V ₊ = 10.8V		40	100	Ω
DYNAMIC						
Turn-On Time	t _{ON}	DG417/DG418, V _D = 8V, Figure 2		110		ns
Turn-Off Time	t _{OFF}	DG417/DG418, V _D = 8V, Figure 2		40		ns
Break-Before-Make Interval	t _D	DG419, R _L = 1000Ω, C _L = 35pF, Figure 4		60		ns
Charge Injection (Note 3)	Q	C _L = 10nF, V _{GEN} = 0V, R _{GEN} = 0V, Figure 5		2	10	pC
SUPPLY						
Positive Supply Current	I ₊	All channels on or off, V ₊ = 13.2V, V _L = 5.25V, V _{IN} = 0V or 5V		-0.0001		μA
Negative Supply Current	I ₋	All channels on or off, V ₊ = 13.2V, V _L = 5.25V, V _{IN} = 0V or 5V		-0.0001		μA
Logic Supply Current	I _L	All channels on or off, V _L = 5.25V, V _{IN} = 0V or 5V		-0.0001		μA
Ground Current	I _{GND}	All channels on or off, V _L = 5.25V, V _{IN} = 0V or 5V		-0.0001		μA

Note 2: Typical values are for **design aid only**, are not guaranteed, and are not subject to production testing. The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: On-resistance match between channels and flatness is guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog range.

Note 5: Leakage parameters I_{S(OFF)}, I_{D(OFF)}, and I_{D(ON)} are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

Note 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D = output, V_S = input to off switch.

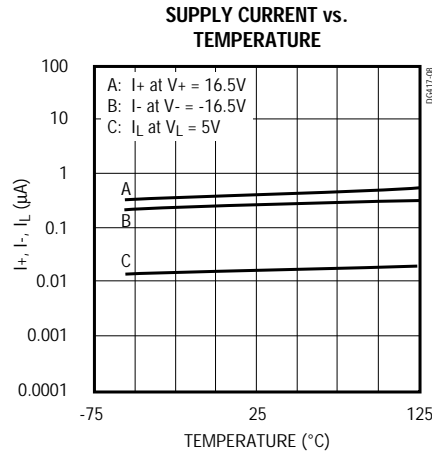
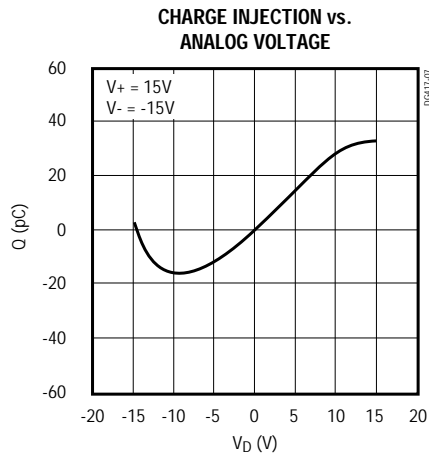
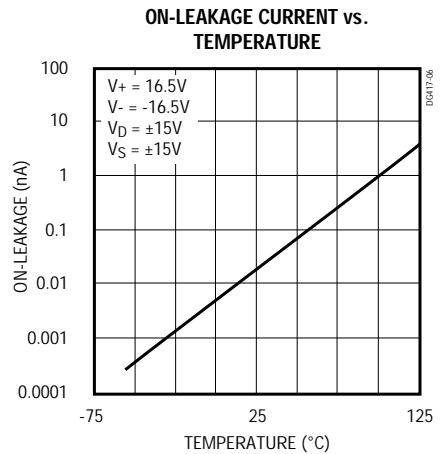
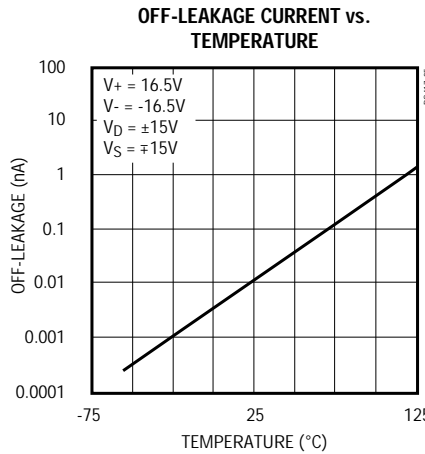
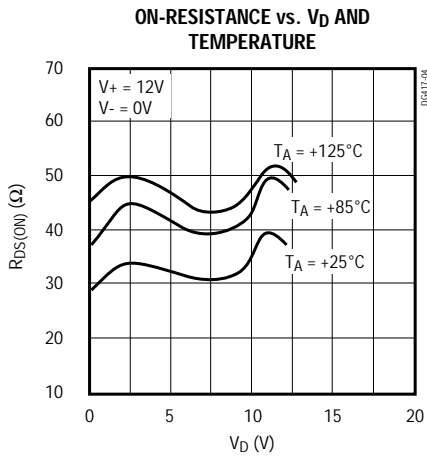
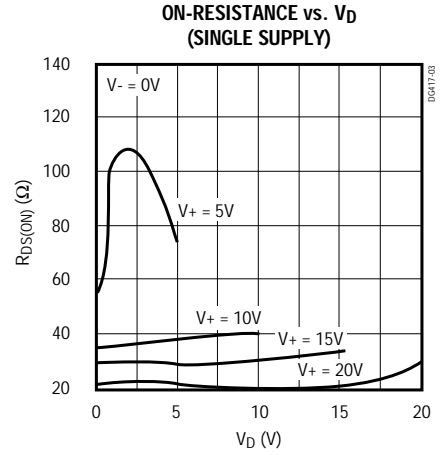
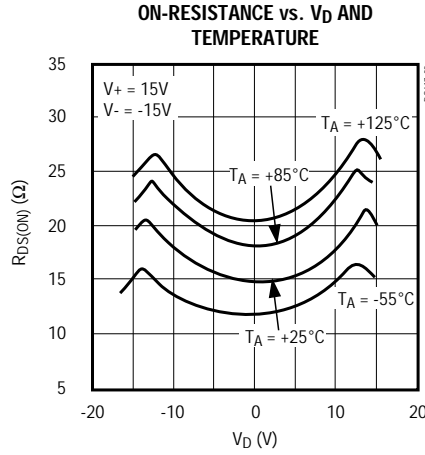
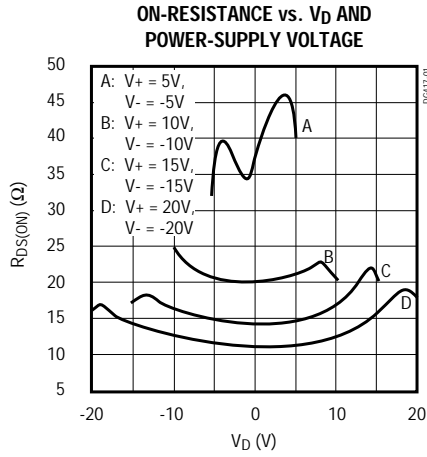
Note 7: Between any two switches.

Improved, SPST/SPDT Analog Switches

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

DG417/DG418/DG419



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Pin Description

PIN			NAME	FUNCTION
DG417	DG418	DG419		
1	—	—	S	Analog-Switch Source Terminal (normally closed)
—	1	—	S	Analog-Switch Source Terminal (normally open)
—	—	2	S1	Analog-Switch Source Terminal 1 (normally closed)
2	2	—	N.C.	No Internal Connection
3	3	3	GND	Logic Ground
4	4	4	V+	Analog-Signal Positive Supply Input
5	5	5	VL	Logic-Level Positive Supply Input
6	6	6	IN	Logic-Level Input
7	7	7	V-	Analog-Signal Negative Supply Input
8	8	1	D	Analog-Switch Drain Terminal
—	—	8	S2	Analog-Switch Source Terminal 2 (normally open)

Applications Information

Operation with Supply Voltages Other than $\pm 15V$

Using supply voltages other than $\pm 15V$ reduces the analog signal range. The DG417/DG418/DG419 switches operate with $\pm 4.5V$ to $\pm 20V$ bipolar supplies or with a $+10V$ to $+30V$ single supply; connect V- to 0V when operating with a single supply. Also, all device types can operate with unbalanced supplies, such as $+24V$ and $-5V$. VL must be connected to $+5V$ to be TTL compatible, or to V+ for CMOS-logic level inputs. The *Typical Operating Characteristics* graphs show typical on-resistance with $\pm 20V$, $\pm 15V$, $\pm 10V$, and $\pm 5V$ supplies. (Switching times increase by a factor of two or more for operation at $\pm 5V$.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by VL, V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with the supply pins for overvoltage protection (Figure 1).

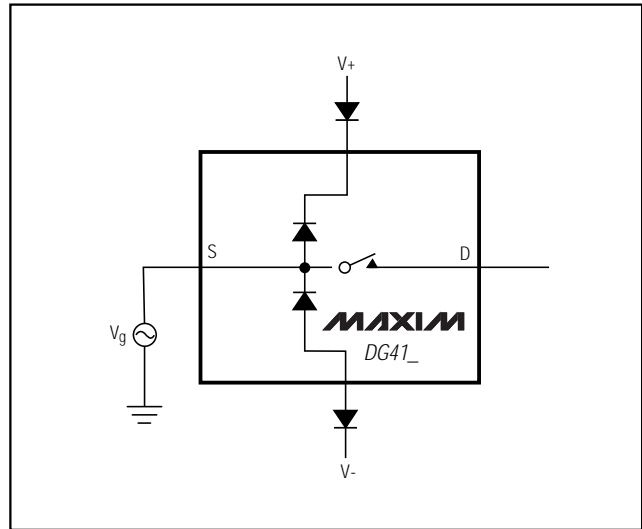


Figure 1. Overvoltage Protection Using External Blocking Diodes

Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, without affecting low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed $+44V$.

Improved, SPST/SPDT Analog Switches

Test Circuits/Timing Diagrams

DG417/DG418/DG419

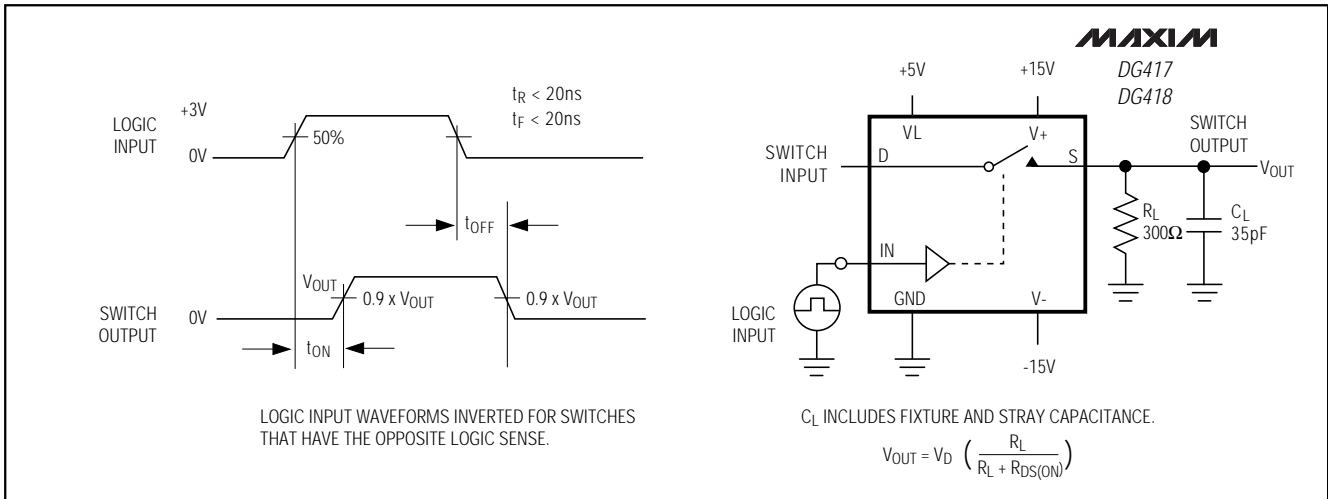


Figure 2. DG417/DG418 Switching Time

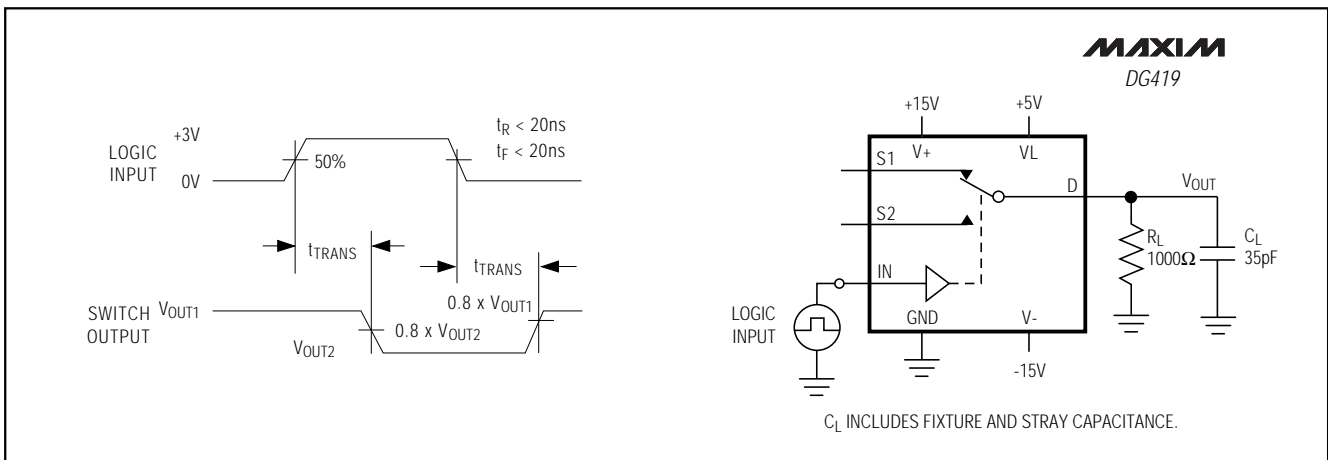


Figure 3. DG419 Transition Time

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Test Circuits/Timing Diagrams (continued)

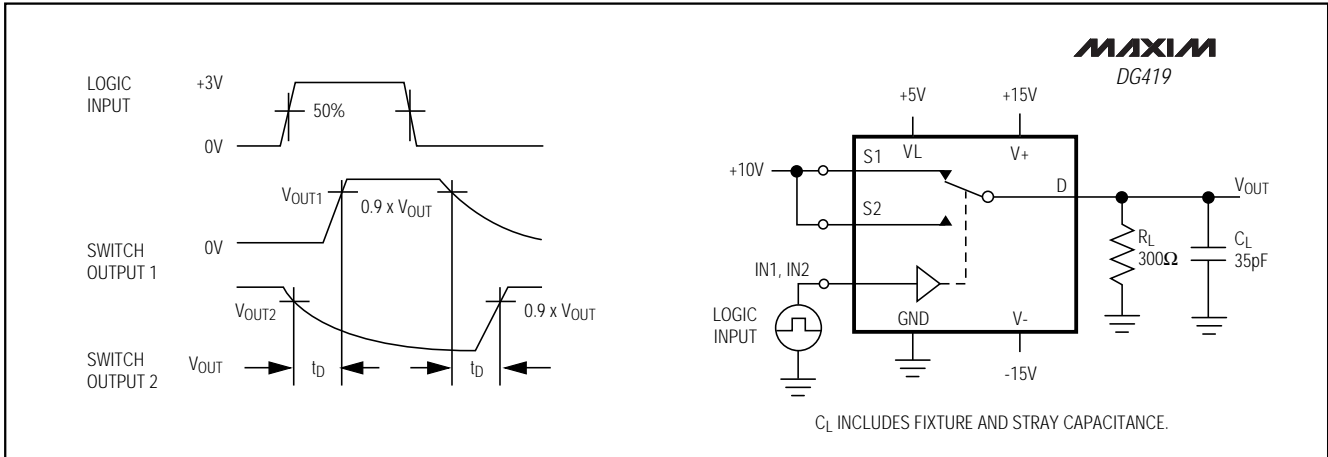


Figure 4. DG419 Break-Before-Make Interval

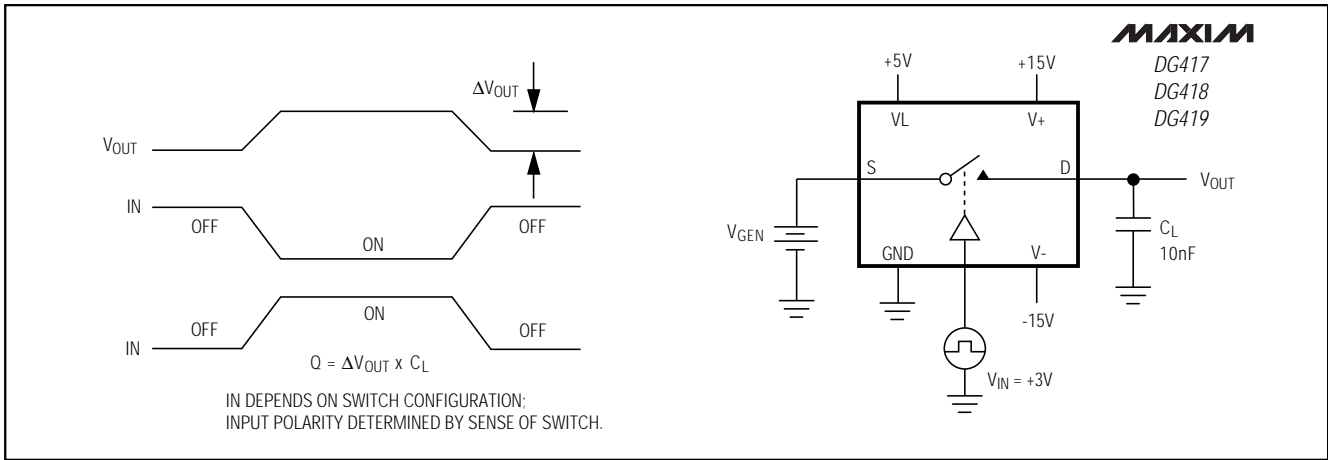


Figure 5. Charge Injection

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Test Circuits/Timing Diagrams (continued)

DG417/DG418/DG419

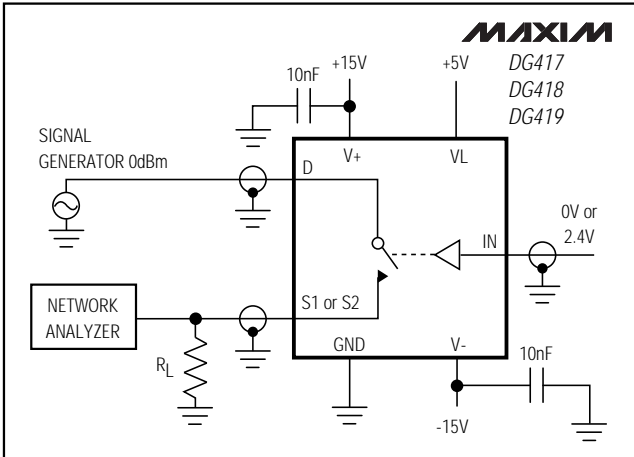


Figure 6. Off-Isolation Rejection Ratio

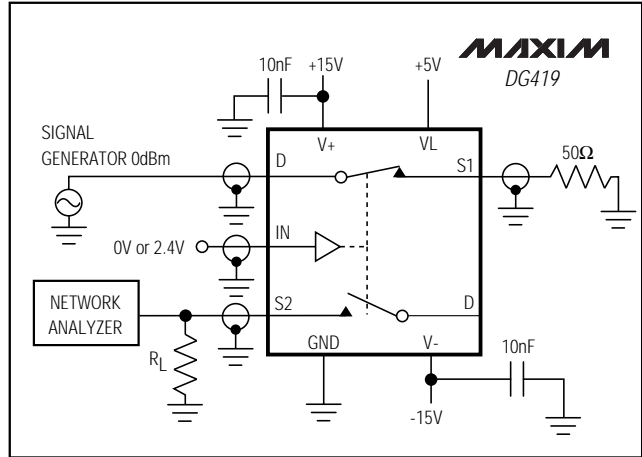


Figure 7. DG419 Crosstalk

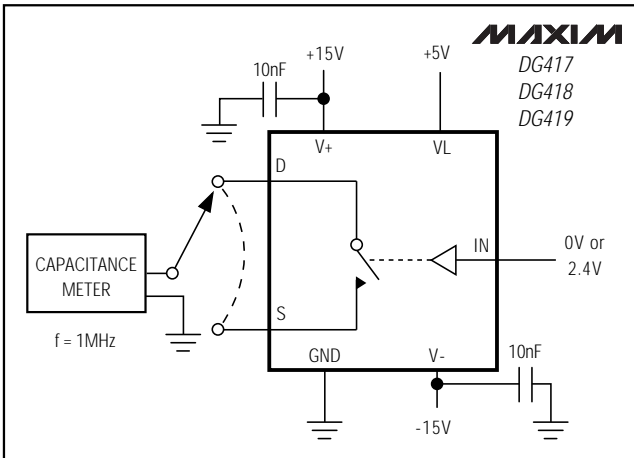


Figure 8. Drain-Source Off-Capacitance

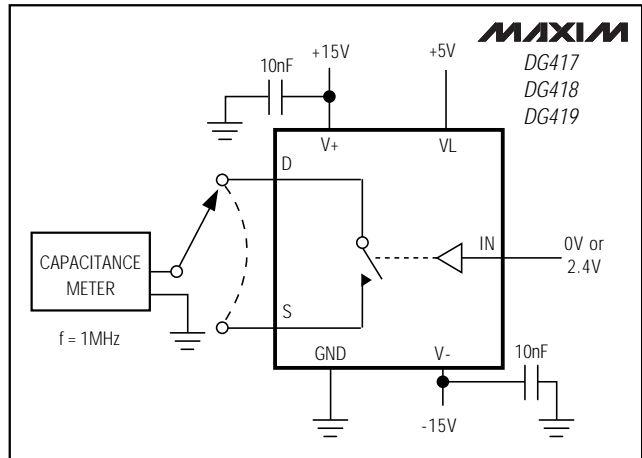


Figure 9. Drain-Source On-Capacitance