Physics 623
Phase Locked Loop

January 16, 2023

1 Prelab Worksheet

Note: Turn in at beginning of lab. If you have any questions about this exercise, please [see, call, email] the instructor well in advance of the lab.

A. Read section 13.13 (pp 955–974) in Horowitz and Hill.

B. In a few sentences, describe the operation of a type I phase detector.

C. In a few sentences, describe the operation of a type II phase detector.

D. Where should pin 5 of the MC14046B P.L.L. chip be connected? (This will require some detective work on the data sheet.)

E. Explain the difference between capture range and lock range for the input frequency.

2 Lab instructions

2.1 Introduction

The phase-locked loop (PLL) is an analog device that uses negative feedback to cause a variable frequency oscillator to adjust itself to either the fundamental or some harmonic of an external AC signal. The device has many interesting applications including frequency synthesis, demodulation of FM and AM signals, frequency multiplication, and pulse synchronization of signals from noisy sources. The device consists of a phase detector(comparator), a filter, and a voltage-controlled oscillator (VCO). In this lab we will use a popular 16 pin package MC14046 which contains, in addition to the VCO, two types of phase detectors (type I and type II) which are level sensitive and edge sensitive respectively. Fig. 1 shows the basic components of the PLL. You need to provide a filter with the desired characteristics between the phase detector output and the VCO input. In your notebook schematic, show the actual filter components between the ϕ-det and VCO blocks, with the proper pin numbers. You can label the capacitor "C_f", since you will be changing its value later.

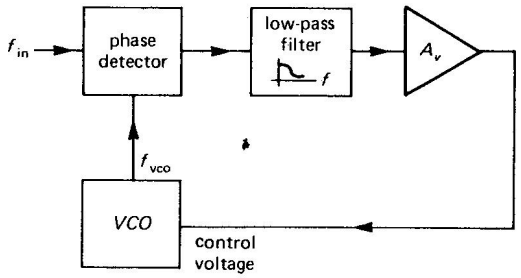

Figure 1: Block Diagram of the PLL.

2.2 The MC14046

The integrated circuit is CMOS. Although higher voltages are possible as detailed by the specification sheet, we will operate our chip from a +5 Volt supply and be careful to maintain TTL logic levels (0-5V) at the input. Use the AFG2021 waveform generator and set the output to a $0 - 4.5V$ square wave. Remember than the 2021 defaults to assuming you want a waveform symmetrical around zero and that you have it connected to a 50-ohm load, neither of which is true. So check the output on your scope *before* you connect it to the chip.

The sensitive FET gates are adequately protected so that you should not need to observe such precautions as a ground strap on your wrist to avoid static discharge. It is a good idea not to apply input signals when there is no DC power on the chip, since this may damage the chip. Since it is easy to forget to disconnect a low-impedance signal

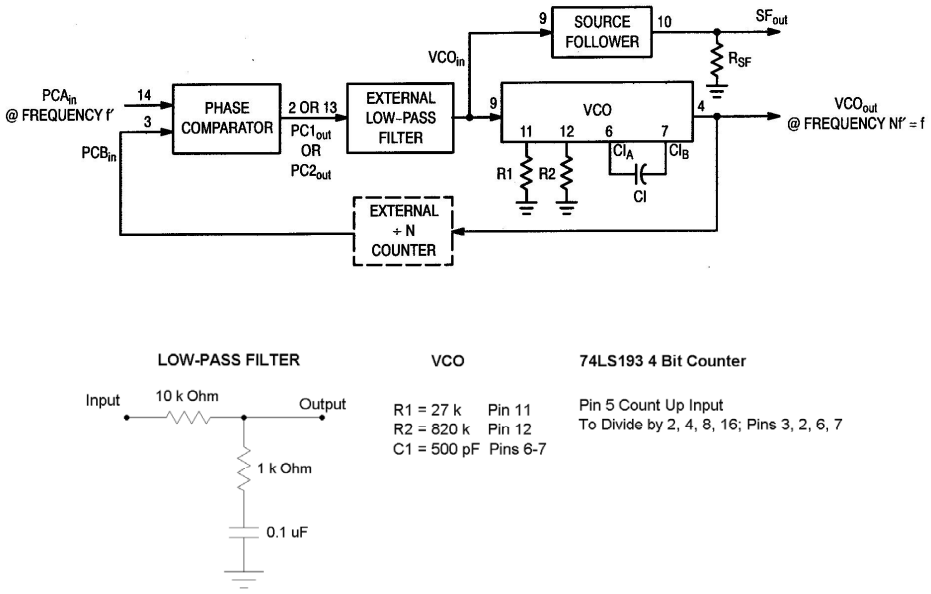

Figure 2: 14046B Block Diagram and Component Values

generator from the input before turning off the power, putting a 560 ohm resistor in series with this input is a good precaution.

The frequency range of the VCO is set by resistors R1 and R2 and capacitor C1, determining f_{min} and f_{max}. The frequency range of the input signal on which the loop will stay locked if it was initially in lock is called the Lock frequency range: $2f_L = f_{max} - f_{min}$. The frequency range of the input signal on which the loop will lock if it was initially out of lock is called the Capture frequency range: $2f_C$. For the Type I comparator $f_C \leq f_L$ while for the Type II comparator, $f_C = f_L$. The Type I is capable of locking on harmonics of the center frequency while the Phase II will not lock on harmonics.

The circuit has a high impedance source follower (SF) which allows one to monitor the input to the VCO even when the filter has a very high impedance. However, this introduces a significant offset, so ignore the SF and just connect your scope to the filter output/VCO input. (You do not need R_{SF} nor any connection to pin 10.)

2.3 Experiment

1. Connect your chip in a standard Phase Lock Loop configuration as shown in Fig. 2. You have to add the R and C external components for the low-pass filter and the VCO.

   Before you begin, disconnect the VCO input from the filter and connect it to an adjustable voltage source (the small white $\pm 5V$ or $\pm 9V$ adjustable power supply is good for this), and make a quick plot in your notebook of f_{out} vs V_{in} for $V_{in} = 0 - 5V$. This will assist you in understanding the operation of the phase locked loop.

Initially use the Type I phase comparator output from pin 2. In a Phase Locked Loop the AC output of the phase comparator is always fed into a filter to provide a D.C. control voltage for the the VCO. The output of the VCO is then returned to the phase comparator to be compared to the signal input. In general one has to be careful to get the polarity of feedback correct, but in this case there is only one possible connection.

2. Use a +4.5 V square wave at 1-2 kHz for the input and the scope trigger. Vary the frequency over a wide range and observe that the VCO will sometimes synchronously lock in and sometimes run freely out of phase. Note that in the locked condition there is a stable voltage input to the VCO. Once locked in, the input frequency can be varied slowly over a wide range and the VCO will stay locked in phase. However, once the locked condition is lost, the input frequency may need to be adjusted to recapture the locked condition.

3. Distinguish qualitatively between the Lock and Capture frequency ranges The Lock range is generally greater than the Capture range. Make a note of the maximum and minimum frequencies of the lock-in range and the corresponding DC levels of the input to the VCO. Only count locking on the fundamental for the frequency ranges.

4. While still using the XOR output of the Type I phase comparator (pin 2), vary the frequency over the lock-in range and observe how the relative phase between the VCO and the input signal depends on frequency. Explain why this phase variation is necessary if the XOR comparator output is to determine the frequency of the VCO.

5. There are frequencies outside of the normal lock-in range where the VCO and input will lock in phase but where the two frequencies have a harmonic relationship to each other. Locate at least one of the harmonic frequencies and measure the frequency ratio.

6. Switch from the Type I comparator to the Type II comparator (pin 13). The Type II has leading edge sensing logic, provides digital error signals $PC2_{out}$ and LD, and maintains a 0° phase shift between the input signals (PCA_{in} and PCB_{in} independent of duty cycle. The Type II charges an output capacitor for the amount of time that the input signal is on before the VCO and discharges the capacitor for any amount of time the VCO is on before the input signal. Determine the Lock and Capture frequency ranges for the Type II comparator. Convince yourself that it does not lock on harmonics. Check to see if the phase varies between the input signal and the VCO as the frequency is varied over the the lock range.

7. *An obvious application of the PLL is as a frequency-to-voltage converter. The PLL could then be used as a demodulator for a signal that is frequency modulated (FM detector). The modulation frequency would have to be low enough to be passed by the filter.*

Another application of the PLL is frequency multiplication. A highly stable and precise frequency source (represented by our waveform generator input signal) can be multiplied to a precise high frequency. A specific case would be to multiply 30 Hz (frames/sec) by 525 (lines/frame) to produce a trigger for 15,750 horizontal sweep lines per second on a television screen. Or a single crystal oscillator could be multiplied by integers that would step an FM detector through the stations on a radio dial.

To illustrate frequency multiplication, insert a 4-bit synchronous counter (74LS193) in the feedback loop as sketched in figure 2. Continue to use the Type II comparator output from pin 13. Add two 1 μF capacitors in parallel to the 0.1 μF in the low-pass filter. The added capacitance will slow the response time of the PLL to frequency variations, but it will also be less sensitive to short term noise, desirable in this application.

Begin by extracting the counter output from pin 6 in order to divide by 8. Set the signal generator at $\approx$ 2 kHz and search for lock-in by comparing the VCO output at pin 4 to the signal input at pin 14. Use pin 14 to also trigger the scope and expand the scope sweep until you get a good measure of the time jitter between the leading edges of the waveform generator and the VCO outputs. Remove one and then both of the 1 μF capacitors and see if you can measure a change in this jitter.

8. With some care it is possible to observe the classic transient behavior of the PLL as it locks on to a signal. Set up the 2021 in burst mode so it produces about a 200 ms burst of square waves at about 6 kHz (1200 cycles) with a repetition period about 0.6 seconds. The amplitude should remain $\sim$ 4.5 V, starting from zero.

   Trigger the scope with the pulse train and observe the the filter output/VCO input on another channel. To get the trigger to wait for the train to start you will need to turn off auto-trigger ("normal"), and to keep it from triggering again on a pulse in the middle of the train you'll need to set "holdoff" to a little more than the 200 ms length of the train. You should be able to see the asymptotic approach to lock-in. Try 2.1 μF (total) and 0.1 μF in the filter. Compare scaling by 8X with no scaling.